BEE2: a multi-purpose computing platform for radio telescope digital signal processing applications

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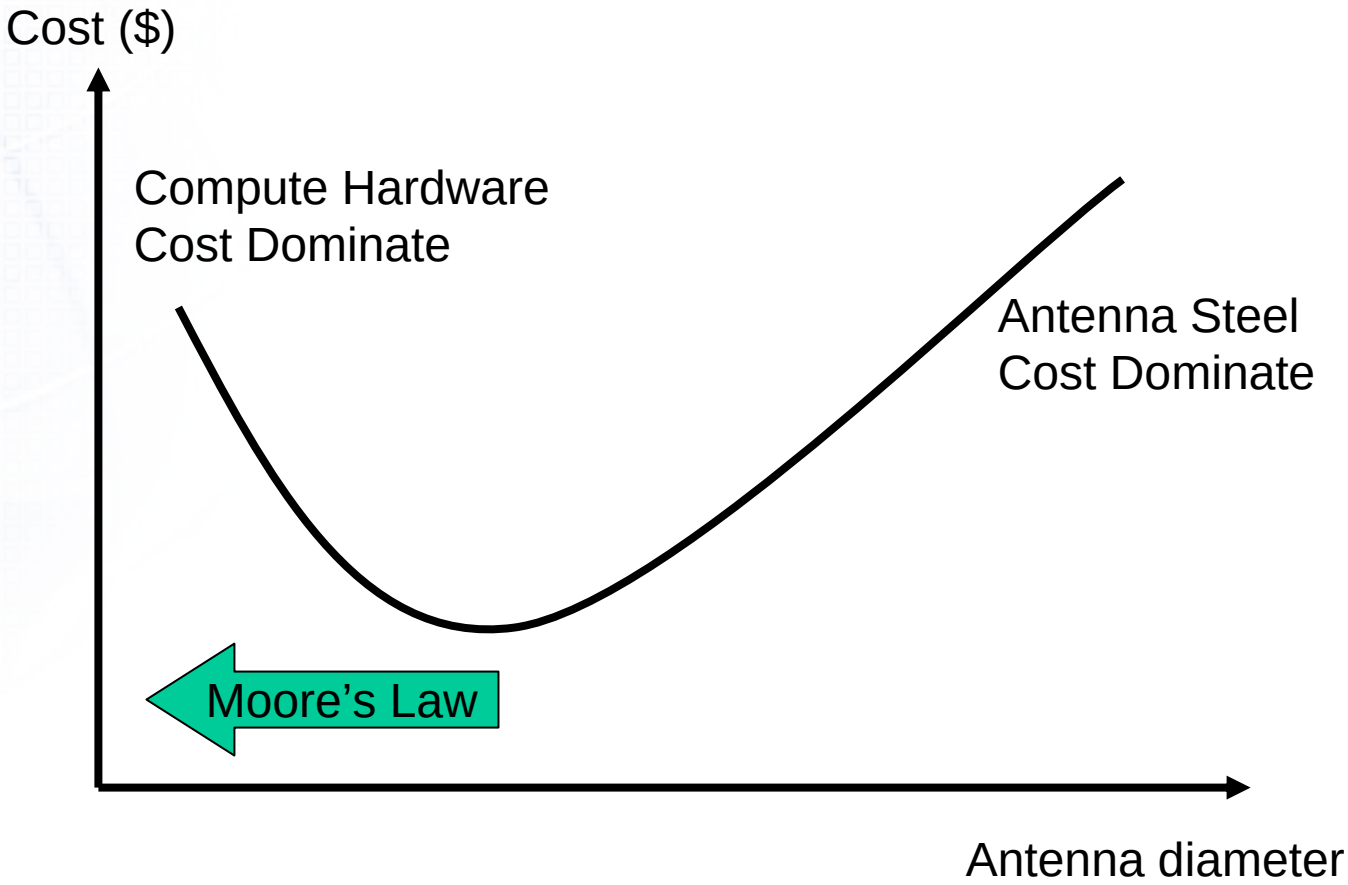
Telescope cost for fixed collect area



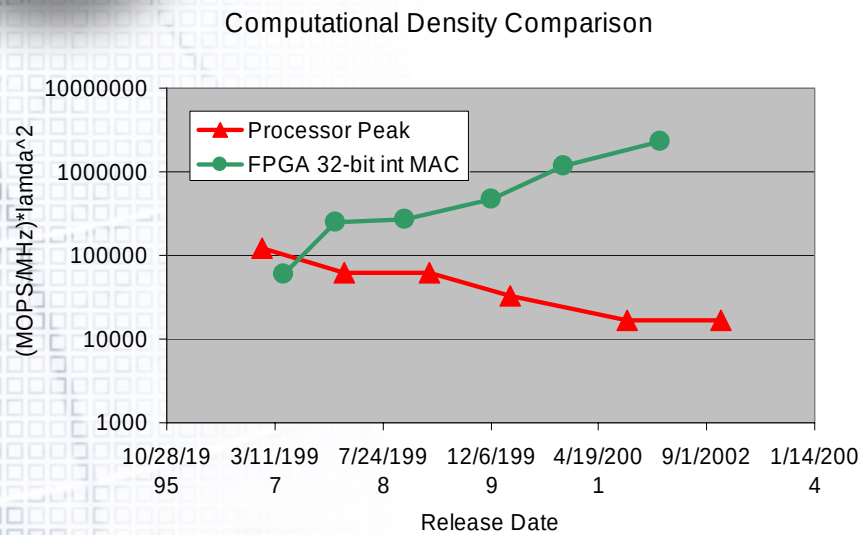
Problems with existing approach

- All specialized instrument design
  - Separate PCB for each subsystem, dedicated functionality
  - Custom interconnect, backplane, and memory interface
  - Fully global synchronous I/O and processing
    - Clock distribution, power consumption, and voltage regulation
- Each instrument design cycle is 5 years!!!
- Instrument upgrade takes the similar effort as designing a new product

Why not use…

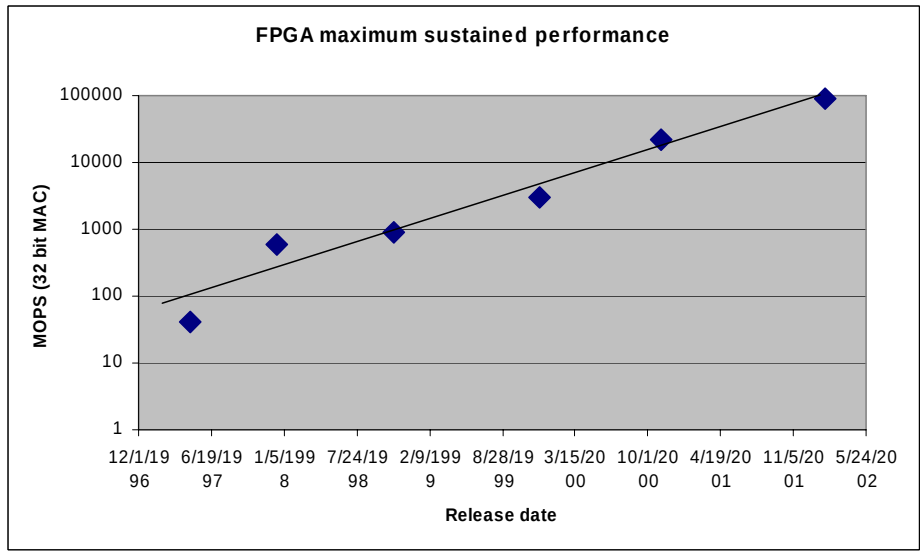
- Microprocessor/DSP clusters?
  - Multi-processor programming is extremely hard, especially for real-time applications
  - Limited I/O capability, high power consumption, low computational density
- ASIC?
  - Lack of flexibility
  - Long design cycles
- FPGA? Sure!

Moore's Law in FPGA world



100X More efficient than micro-processors!

3X improvement per year!

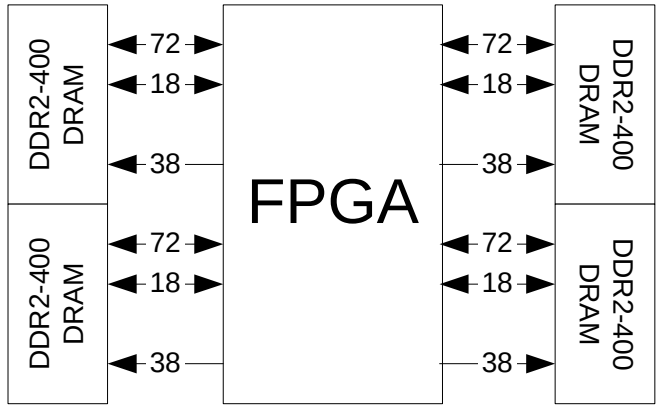


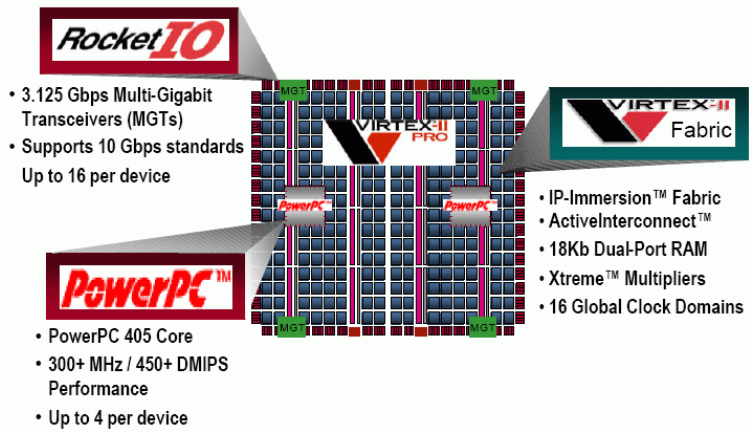
BEE2 system design philosophy

- Compute-by-the-yard
  - Modular computing resource
  - Flexible interconnect architecture
  - On-demand reconfiguration of computing resources
- Economy-of-scale
  - Ride the semiconductor industry Moore's Law curve
  - All COTS components, no specialized hardware
  - Survival of application software using technology independent design flow

Basic Computing Element

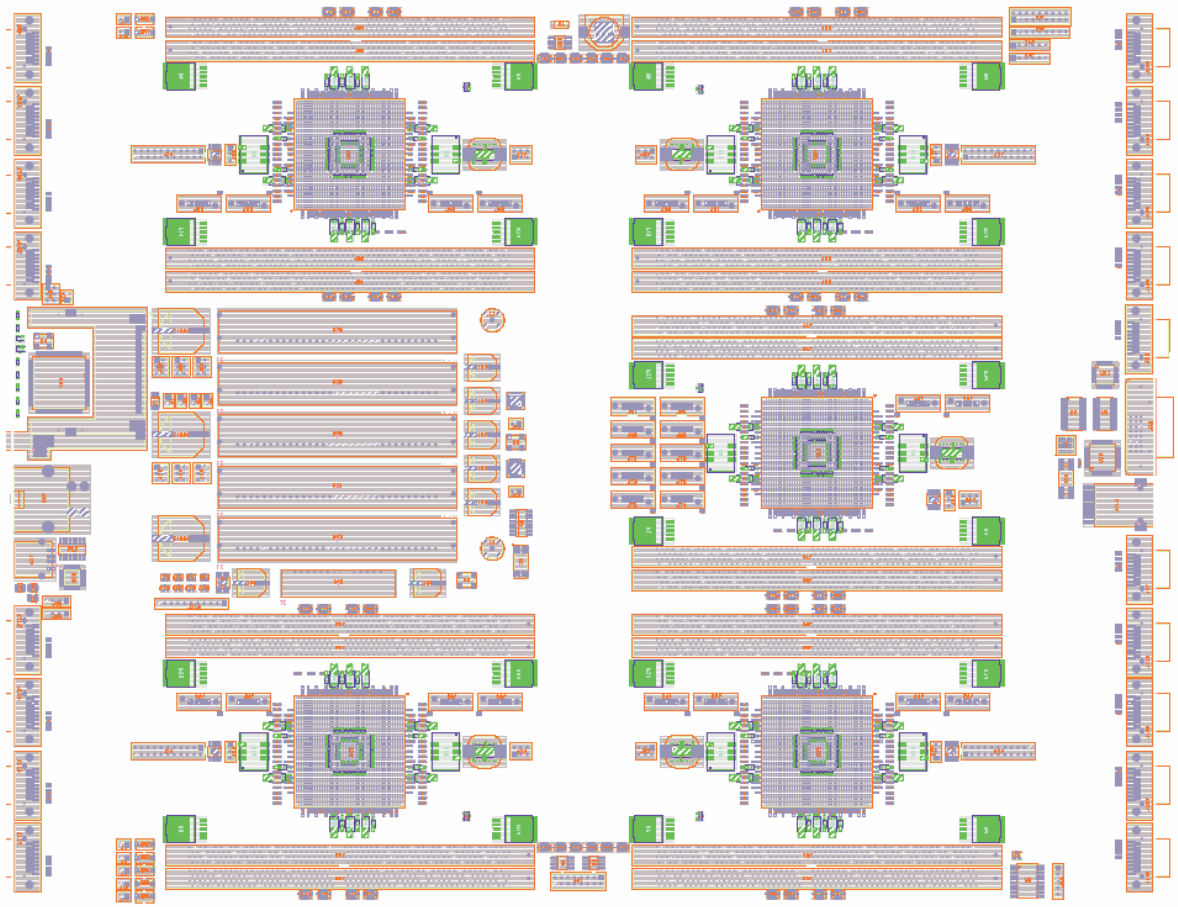
- Single Xilinx Virtex 2 Pro 70 FPGA
  - ~70K logic cells
  - 2 PowerPC405 cores
  - 326 dedicated multipliers (18-bit)
  - 5.8 Mbit on-chip SRAM
  - 80 Gbps MGT I/O bandwidth
  - Over 80 billion CMac/s performance
- 4 physical DDR2-400 banks
  - Each banks has 72 data bits with ECC
  - Independently addressed with 32 banks total
  - Up to 12.8 GBps memory bandwidth, with maximum 8 GB capacity





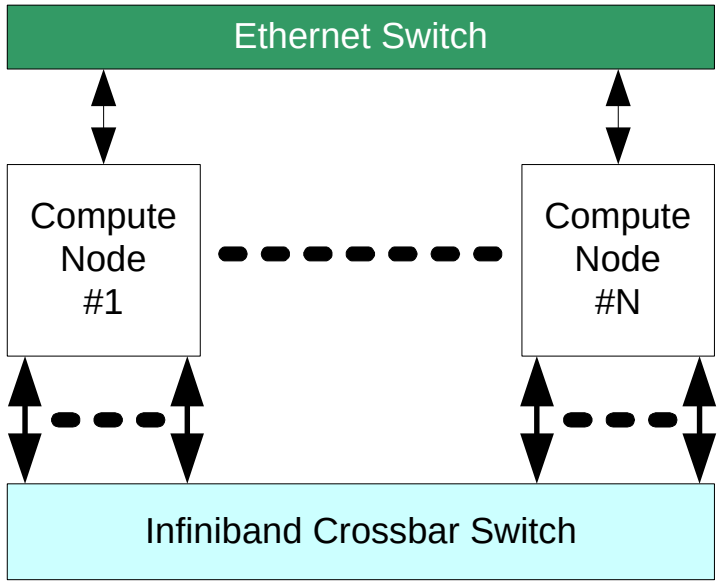
B2 Module: board layout

- 5 compute elements on a board
- Up to 400 billion CMAC/s performance
- communication bandwidth:
  - 240 Gbps on-board
    360 Gbps off-board
- Module:
  - 14X17 inch 22 layer PCB
  - Hardware cost per module: $20K



Global Interconnects

- Commercial Infiniband switch from Mellanox, Voltaire, etc.
  - Packet switched, non-blocking
  - 24 ~ 144 ports (4X) per chassis
  - Up to 10,000 ports in a system
  - 200~1000 ns switch latency
  - 400~1200 ns FPGA to FPGA latency
  - 480Gbps ~ 2.88Tbps full duplex constant cross section bandwidth
  - <$400 per port
- Ethernet
  - Administrative usage only
  - System monitoring
  - Debugging

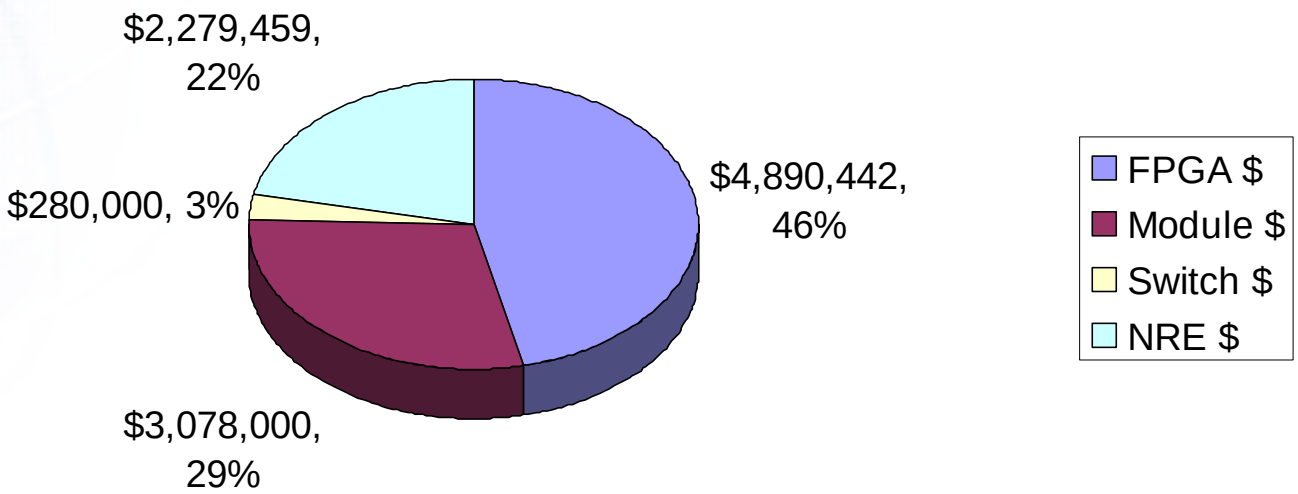


19” 48RU Rack Cabin Capacity

- 40 compute nodes in 5 chassis (8U) per rack
- Up to 16 trillion CMac/s performance per rack
- 250 Watt AC/DC power supply to each blade
- 12.5 Kwatt total power consumption
- Hardware cost: ~ $1M

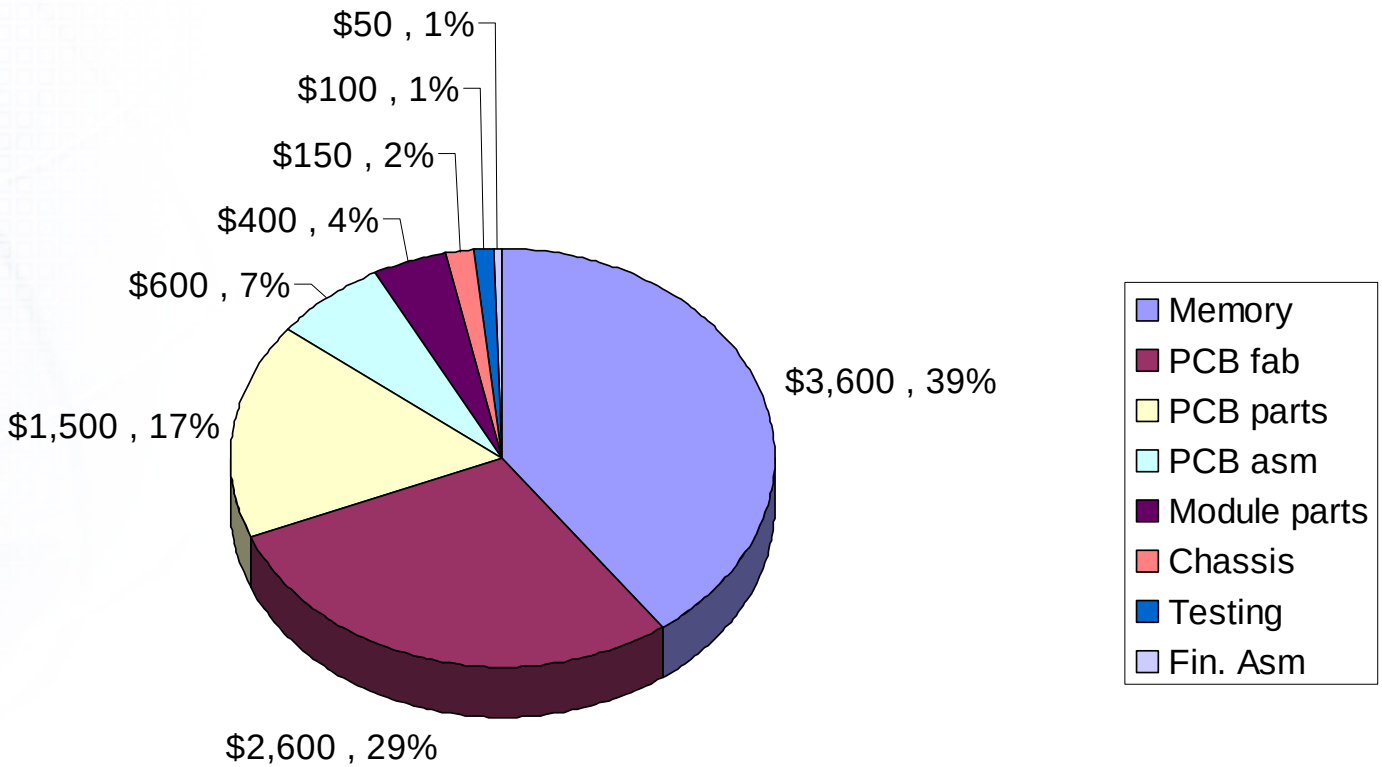
BEE2 system cost breakdown

For 100 Trillion CMAC/s performance
Using 342 BEE2 modules, 14 Infiniband switches
Total system cost with NRE: $10 Million USD



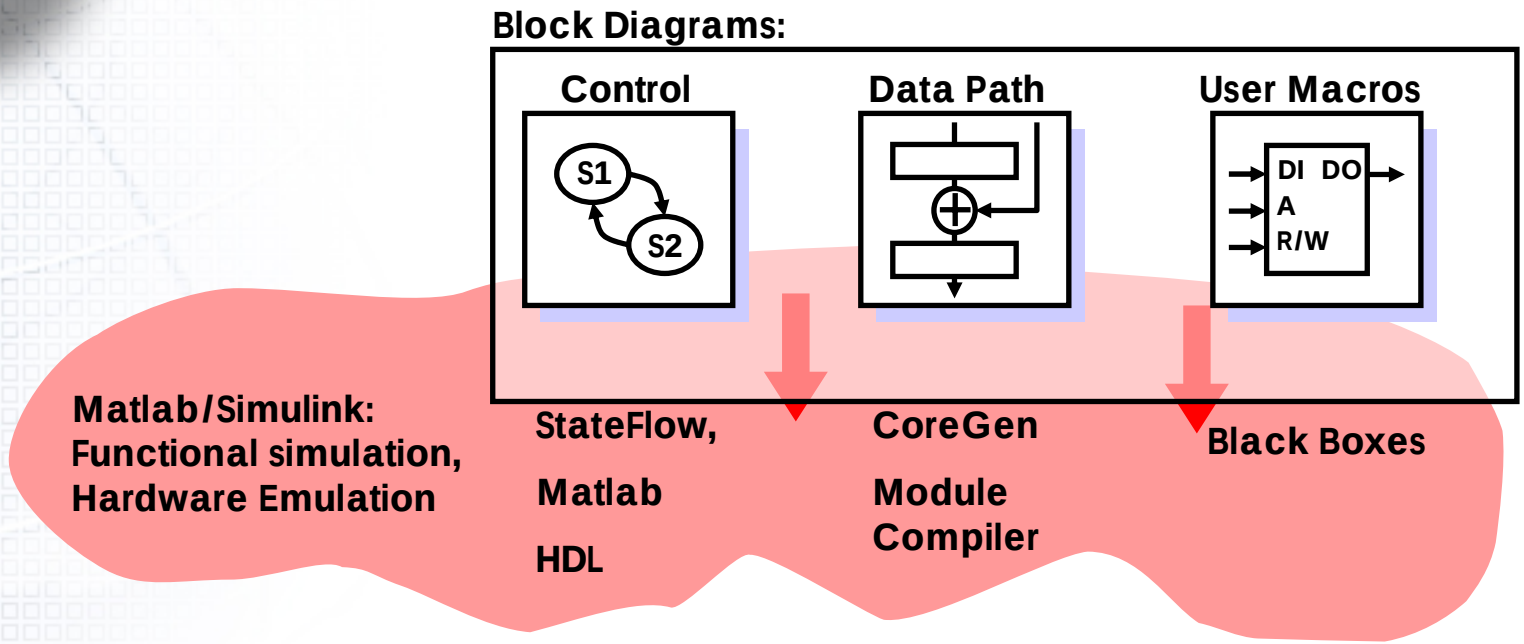
NRE cost includes algorithm ,PCB design, hardware mapping, system integration and testing.

BEE module cost breakdown



Not including FPGA cost

Programming Model :
Discrete Time Block Diagram with FSM

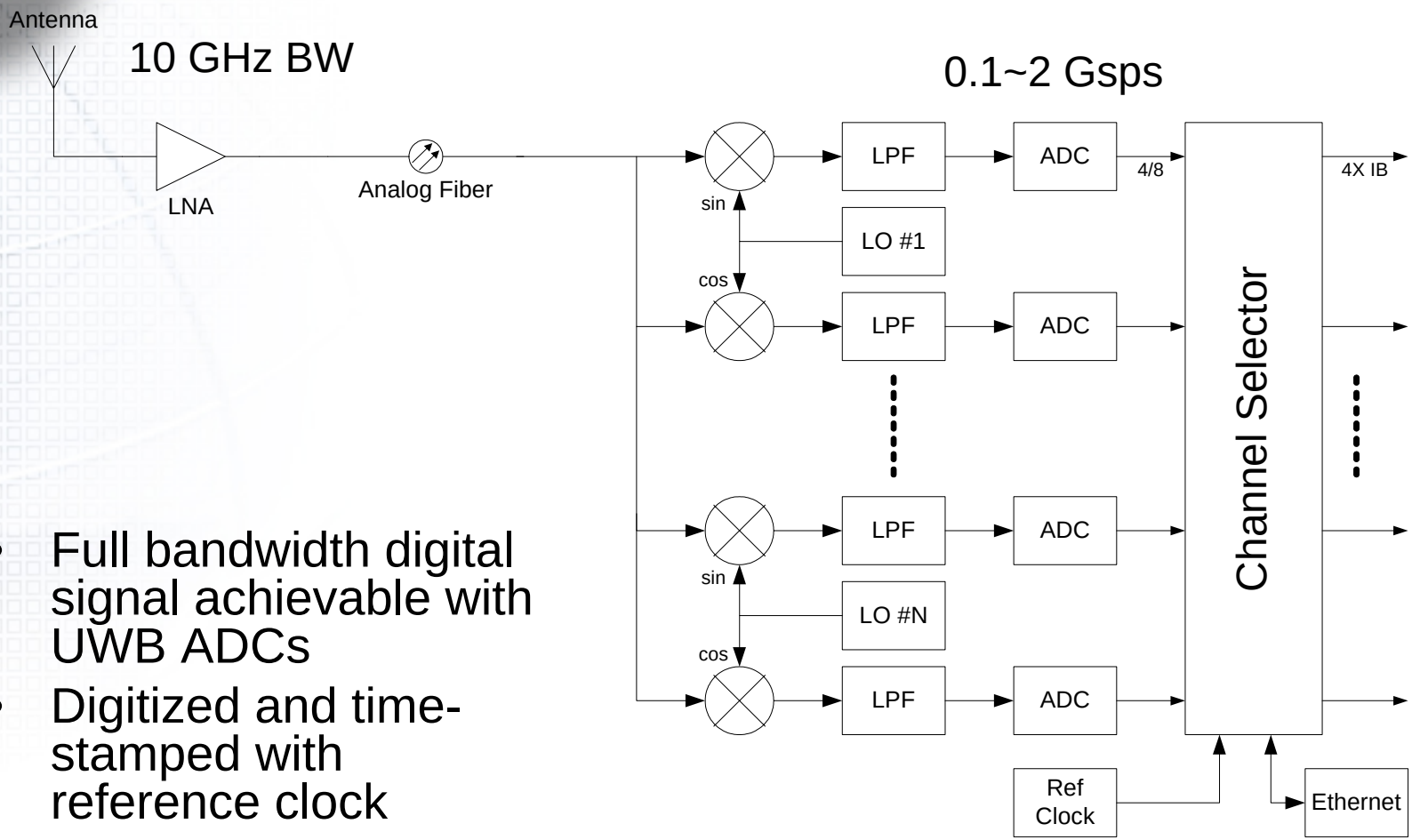


- Xilinx system generator library with BEE2 hardware specific hardware abstractions
- User assisted portioning with automatic system level routing

BEE2 hardware abstractions

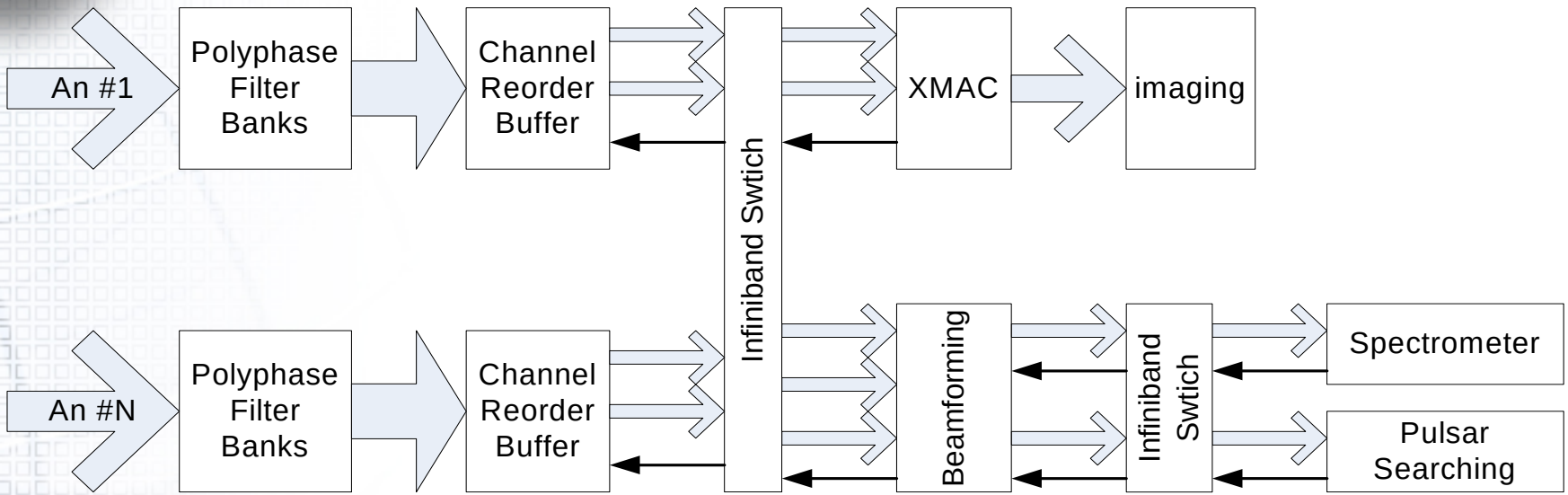
- Data flow operators
  - Data type: fix-point
  - Math operators: +/-, *, /, &, |, xor, ~, >, =, <, srl, sll, sra
  - Control operators: demux/switch, mux/merge
- Memory
  - On-chip SRAM/Registers: shift register, RAM, ROM
  - Off-chip DRAM: stream RAM
- Communication and I/O
  - Static links: stream I/O
  - Dynamic links: Remote DMA
- Synchronization
  - Time stamp

Direct conversion radio frontend



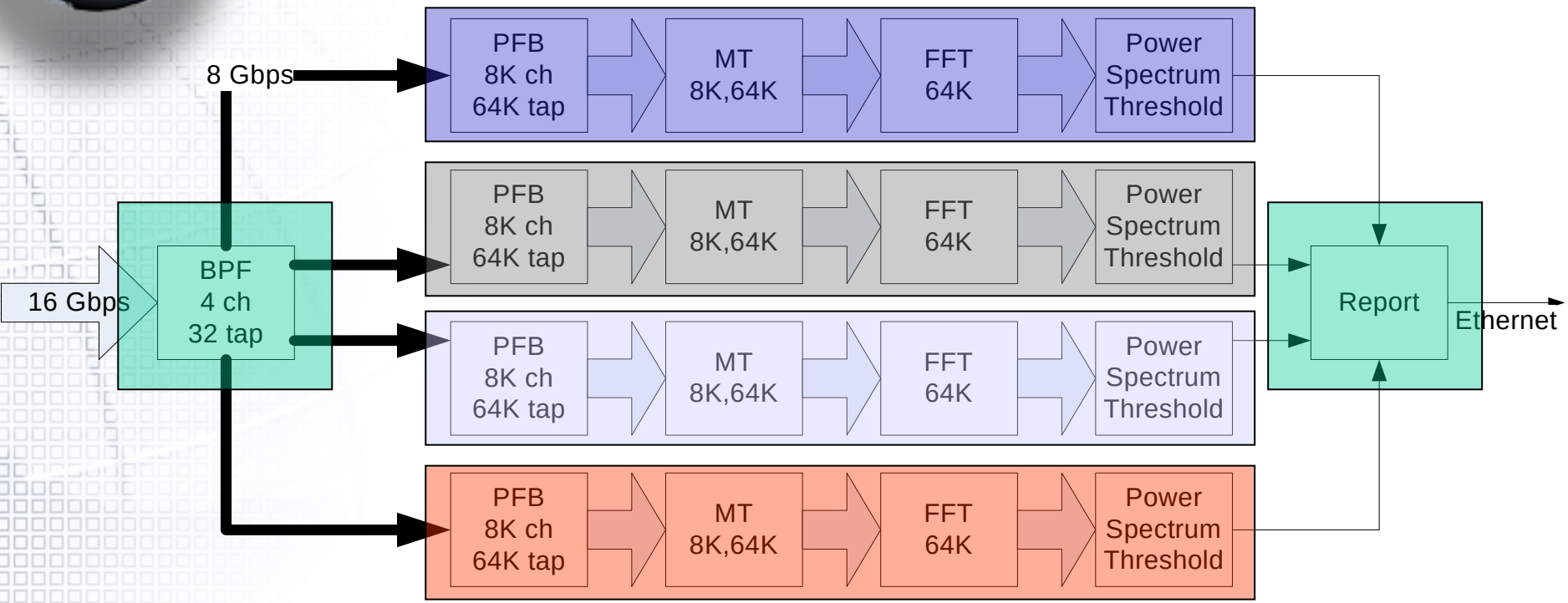
- Full bandwidth digital signal achievable with UWB ADCs
- Digitized and time-stamped with reference clock

Unified Digital Processing Architecture



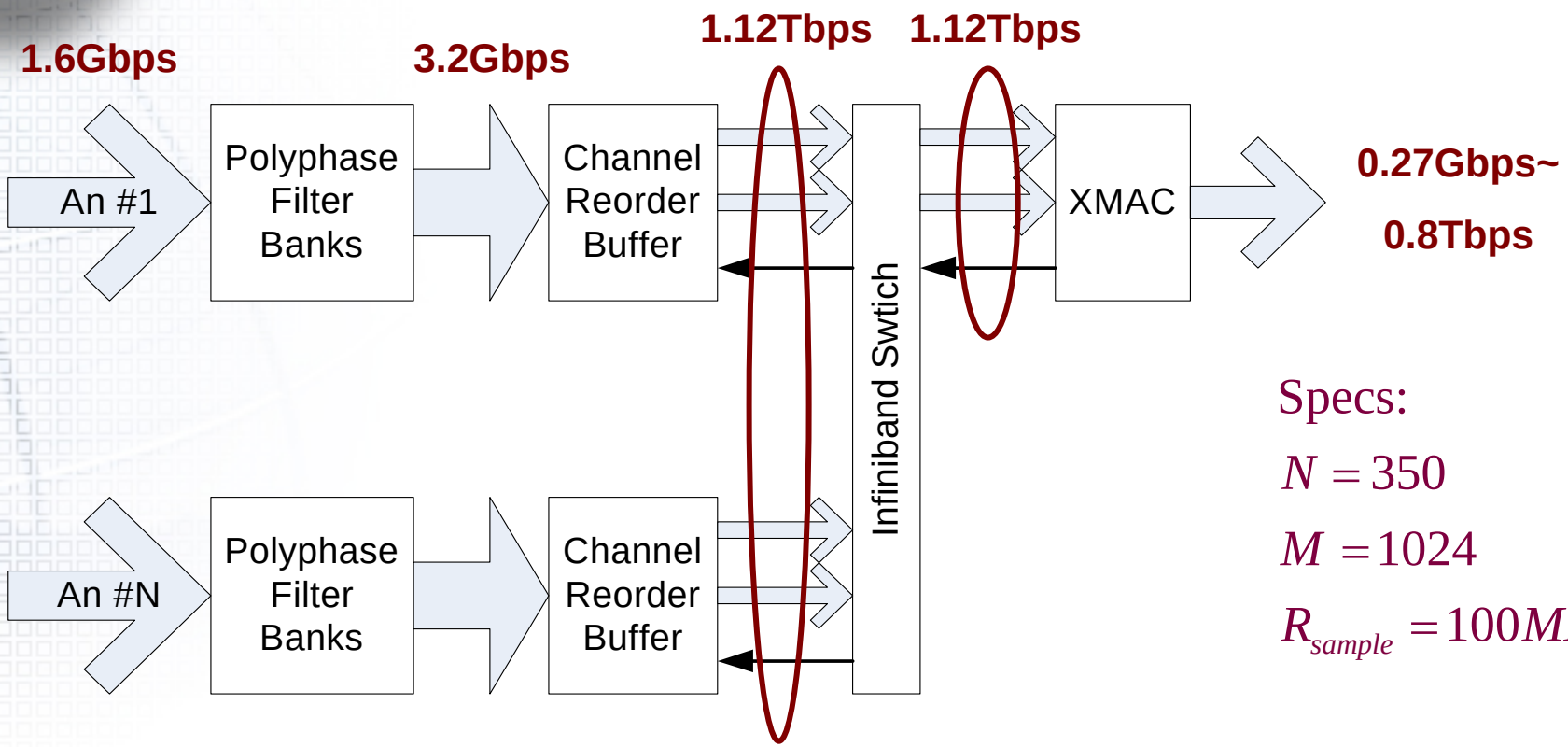
- Distributed per antenna spectral channel processing
- Multiple reconfigurable backend application processing
- Commercial packet switched interconnect
- Backend data pulling through remote DMA access
- Locally synchronous, global asynchronous

1 GHz 2 billion channel spectrometer



- 1 GHz input bandwidth (dual polarization, 4 bit I & Q)
- 2 billion channel spectrometer (0.465 Hz resolution)
- In a single BEE2 module

FX Correlator (ATA350, single IF) in 144 BEE2 modules



Specs:

$N = 350$

$M = 1024$

$R_{sample} = 100MHz$

44 BEE2 modules for PFB & CRB
100 BEE2 modules for XMAC
Single 144 port Infiniband switch

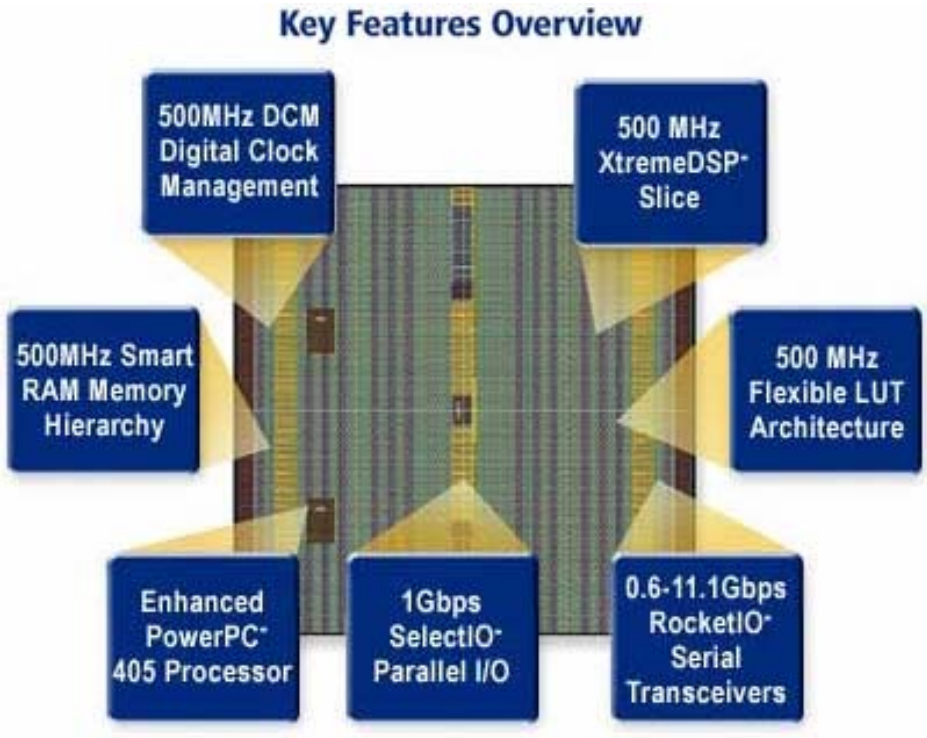
Input Bitwidth = 4, 4
Polarization = 2
Dump time = $10ms \sim 30s$
Output Bitwidth = 32

Current status and projected timeline

- BEE2 PCB schematic design (5/2004, finished)
- BEE2 PCB layout design (8/2004, on going)
- First prototype system of 2 compute nodes tested and operational (12/2004)
- 12 node system manufacturing (2005, H1)
- Demonstration of 32 antenna correlator, 16 pt beamforming, and 1 GHz 2B ch spectrometer (2005, H2)

Future: BEE3 in 2007

- Xilinx just announced Virtex-4 family
  - 4~6X performance improvement
- DDR2 Memory specification up to 800MHz, 4GB per DIMM
- 100 Gbps Infiniband specification under development
- Direct scaling of BEE2 architecture



Scaling of the BEE2 architecture

Radio Telescope	ATA 350	SKA 2000	SKA 4400
Total IF bandwidth in GHz	0.4	2	4
Antennas	350	2000	4400
Beam	16	128	512
Correlator comp. req. (CMac/s)	4.9E+13	8E+15	7.744E+16
Beamformer comp. req. (CMAC/s)	8.96E+12	2.048E+15	3.60448E+16
BEE2 cost in $M (1X, 2005)	$ 6.10	$ 1,057.84	$ 11,947.57
BEE3 cost in $M (5X, 2007)	$ 1.22	$ 211.57	$ 2,389.51
BEE4 cost in $M (25X, ~2009)	$ 0.24	$ 42.31	$ 477.90
BEE5 cost in $M (125X, ~2011)	$ 0.05	$ 8.46	$ 95.58

The BEE2 Team

- Faculty in charge
  - *Bob W. Brodersen*
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- Graduate students
  - *Kevin Camera*
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  - *Alexander Krasnov*
  - *Yury Markovskiy*
  - *Adam Megacz*
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- Industrial Liaison
  - *Ivo Bolsens (Xilinx)*
  - *Bob Conn (Xilinx)*
- Research associates
  - *Don Becker (UCB, astro)*
  - *Dan Werthimer (SSL)*
  - *Melvyn Wright (UCB, RAL)*
- Technical staff
  - *Susan H. Mellers*
  - *Brian Richards*
- Undergraduate student
  - *John Conner*
  - *Greg Gibeling*