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BEE2 GROUP
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NOTES
BEE2 MOTHERBOARD
SIDE **D**
SHEET 1 OF 65

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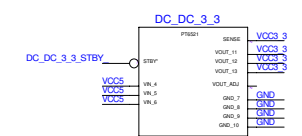
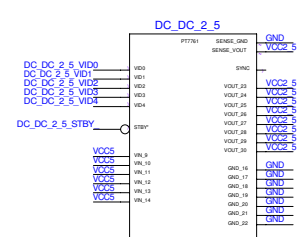
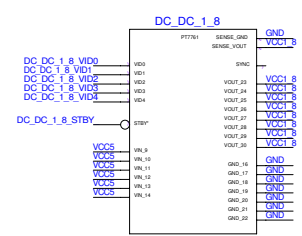
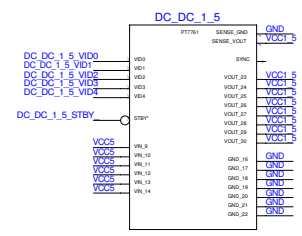
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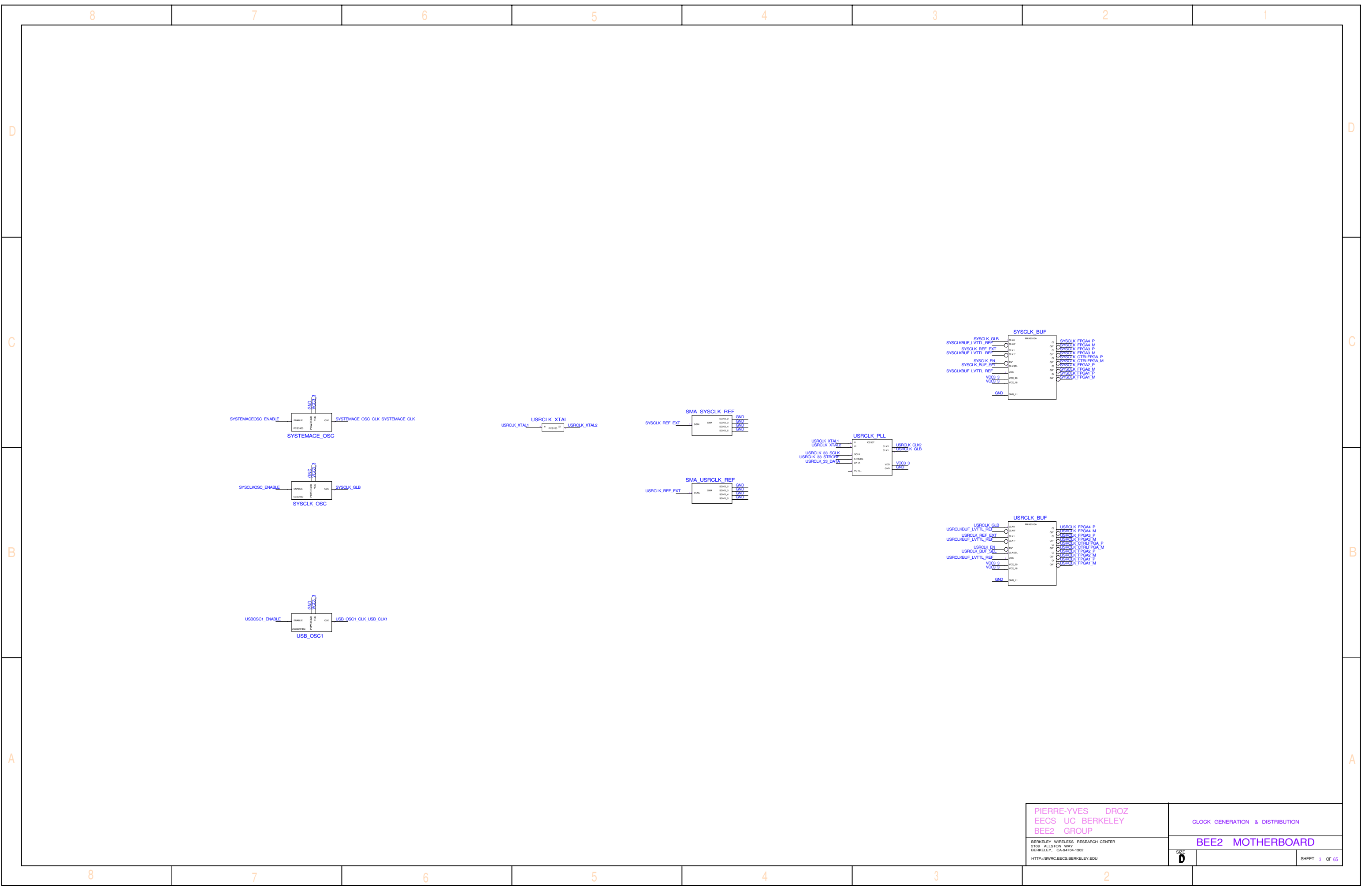
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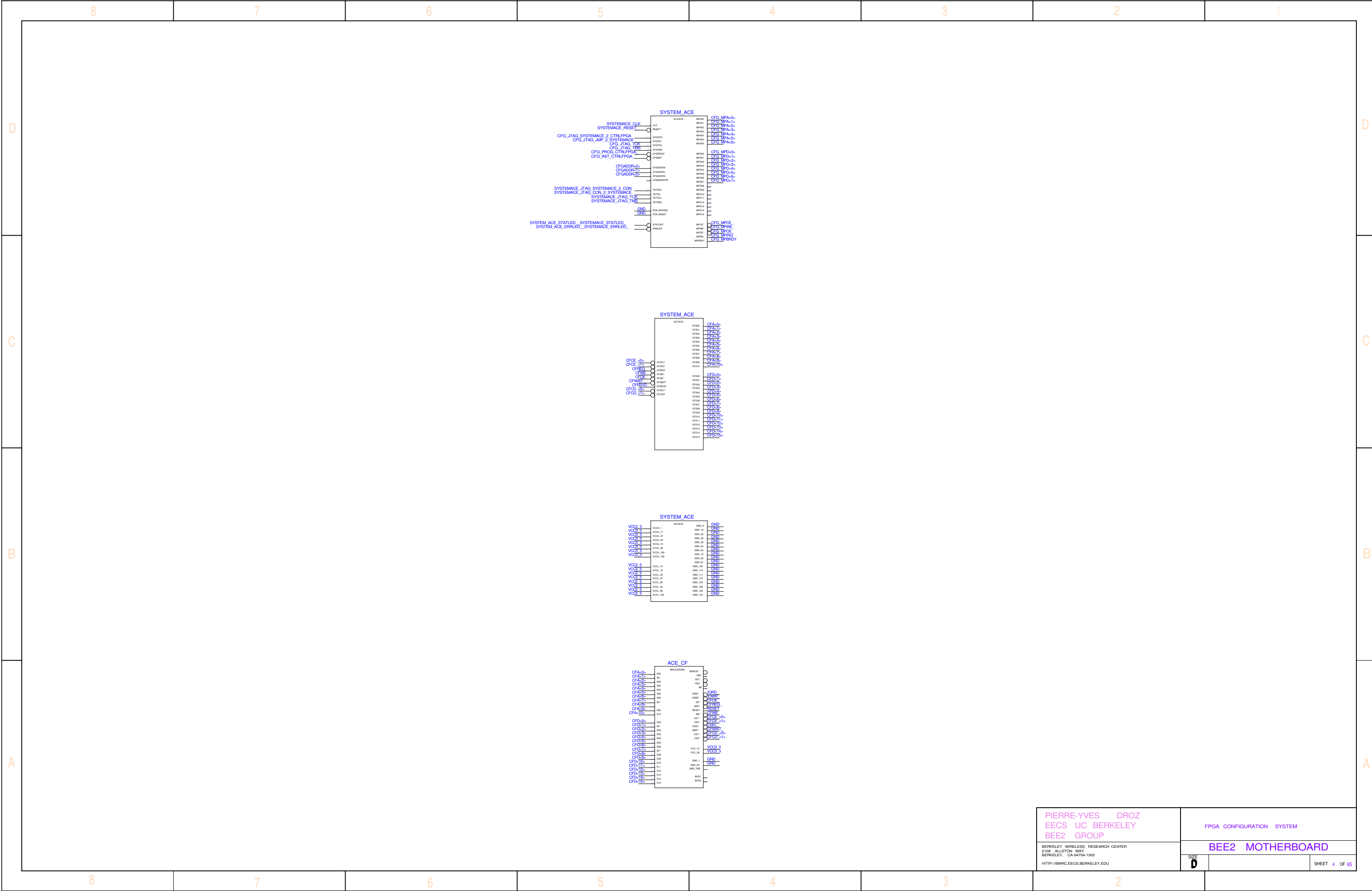
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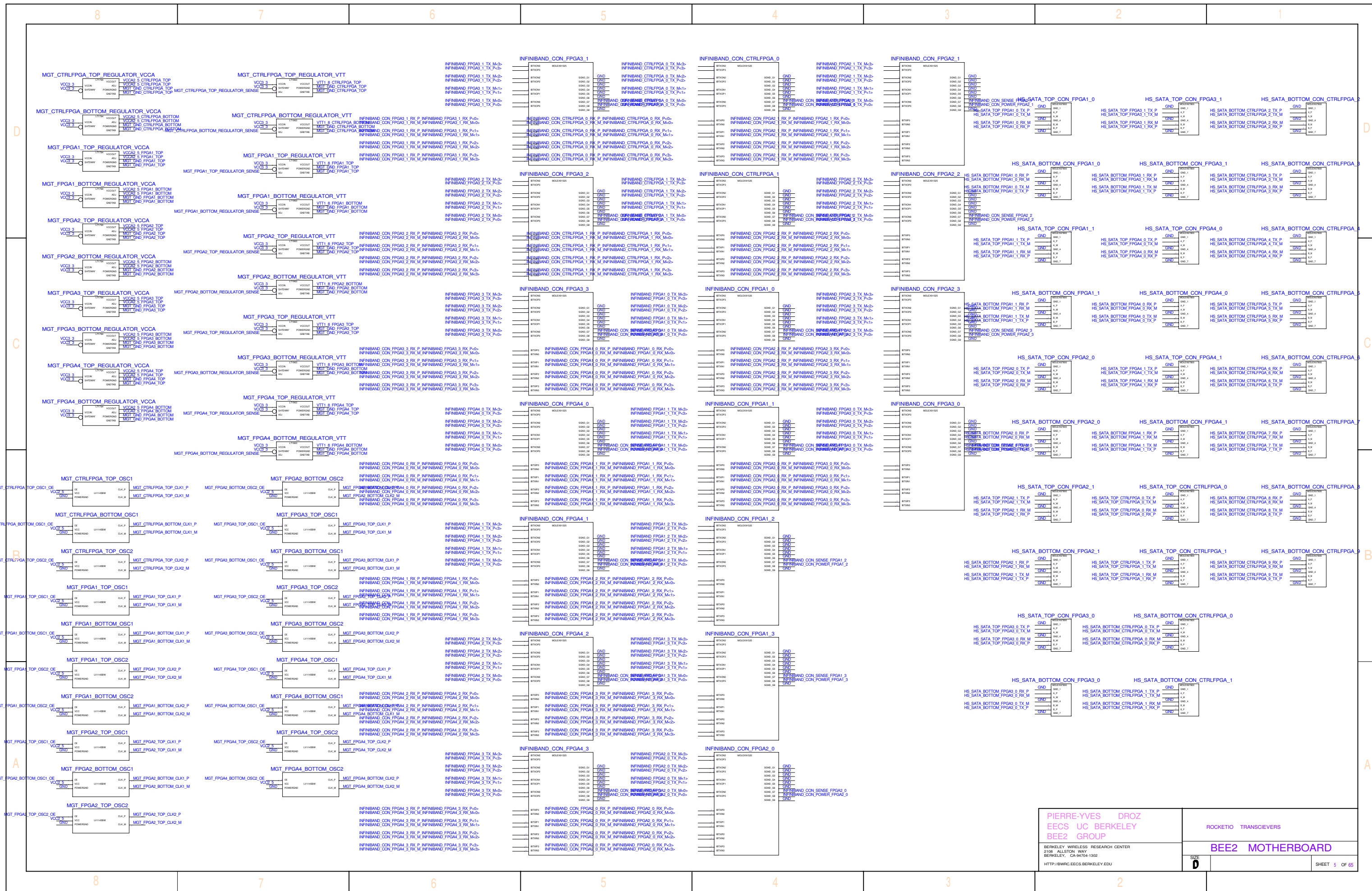
CLOCK GENERATION & DISTRIBUTION

BEE2 MOTHERBOARD

SIDE
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SHEET 3 OF 65





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SIZE
D

SHEET 5 OF 65

DDR2_CTRLFPGA_1

Table of DDR2_CTRLFPGA_1 signals including DDR2CTRLFPGA_1_DQ0-15, DDR2CTRLFPGA_1_DM0-3, DDR2CTRLFPGA_1_A0-13, DDR2CTRLFPGA_1_BA0-1, DDR2CTRLFPGA_1_WE, DDR2CTRLFPGA_1_TAS, DDR2CTRLFPGA_1_CAS, DDR2CTRLFPGA_1_S_0b, DDR2CTRLFPGA_1_S_1c, DDR2CTRLFPGA_1_ODT0b, DDR2CTRLFPGA_1_ODT1c, DDR2CTRLFPGA_1_CKE, DDR2CTRLFPGA_1_KE, DDR2CTRLFPGA_1_OK_P0b, DDR2CTRLFPGA_1_OK_P1c, DDR2CTRLFPGA_1_OK_M1b, DDR2CTRLFPGA_1_OK_M2c, DDR2CTRLFPGA_1_RESET, DDR2CTRLFPGA_1_C8b-7, DDR2CTRLFPGA_1_DQS0-8.

DDR2_CTRLFPGA_3

Table of DDR2_CTRLFPGA_3 signals including DDR2CTRLFPGA_3_DQ0-15, DDR2CTRLFPGA_3_DM0-3, DDR2CTRLFPGA_3_A0-13, DDR2CTRLFPGA_3_BA0-1, DDR2CTRLFPGA_3_WE, DDR2CTRLFPGA_3_TAS, DDR2CTRLFPGA_3_CAS, DDR2CTRLFPGA_3_S_0b, DDR2CTRLFPGA_3_S_1c, DDR2CTRLFPGA_3_ODT0b, DDR2CTRLFPGA_3_ODT1c, DDR2CTRLFPGA_3_CKE, DDR2CTRLFPGA_3_KE, DDR2CTRLFPGA_3_OK_P0b, DDR2CTRLFPGA_3_OK_P1c, DDR2CTRLFPGA_3_OK_M1b, DDR2CTRLFPGA_3_OK_M2c, DDR2CTRLFPGA_3_RESET, DDR2CTRLFPGA_3_C8b-7, DDR2CTRLFPGA_3_DQS0-8.

DDR2_FPGA_1

Table of DDR2_FPGA_1 signals including DDR2FPGA1_DQ0-15, DDR2FPGA1_DM0-3, DDR2FPGA1_A0-13, DDR2FPGA1_BA0-1, DDR2FPGA1_WE, DDR2FPGA1_TAS, DDR2FPGA1_CAS, DDR2FPGA1_S_0b, DDR2FPGA1_S_1c, DDR2FPGA1_ODT0b, DDR2FPGA1_ODT1c, DDR2FPGA1_CKE, DDR2FPGA1_KE, DDR2FPGA1_OK_P0b, DDR2FPGA1_OK_P1c, DDR2FPGA1_OK_M1b, DDR2FPGA1_OK_M2c, DDR2FPGA1_RESET, DDR2FPGA1_C8b-7, DDR2FPGA1_DQS0-8.

DDR2_FPGA_3

Table of DDR2_FPGA_3 signals including DDR2FPGA3_DQ0-15, DDR2FPGA3_DM0-3, DDR2FPGA3_A0-13, DDR2FPGA3_BA0-1, DDR2FPGA3_WE, DDR2FPGA3_TAS, DDR2FPGA3_CAS, DDR2FPGA3_S_0b, DDR2FPGA3_S_1c, DDR2FPGA3_ODT0b, DDR2FPGA3_ODT1c, DDR2FPGA3_CKE, DDR2FPGA3_KE, DDR2FPGA3_OK_P0b, DDR2FPGA3_OK_P1c, DDR2FPGA3_OK_M1b, DDR2FPGA3_OK_M2c, DDR2FPGA3_RESET, DDR2FPGA3_C8b-7, DDR2FPGA3_DQS0-8.

DDR2_CTRLFPGA_2

Table of DDR2_CTRLFPGA_2 signals including DDR2CTRLFPGA_2_DQ0-15, DDR2CTRLFPGA_2_DM0-3, DDR2CTRLFPGA_2_A0-13, DDR2CTRLFPGA_2_BA0-1, DDR2CTRLFPGA_2_WE, DDR2CTRLFPGA_2_TAS, DDR2CTRLFPGA_2_CAS, DDR2CTRLFPGA_2_S_0b, DDR2CTRLFPGA_2_S_1c, DDR2CTRLFPGA_2_ODT0b, DDR2CTRLFPGA_2_ODT1c, DDR2CTRLFPGA_2_CKE, DDR2CTRLFPGA_2_KE, DDR2CTRLFPGA_2_OK_P0b, DDR2CTRLFPGA_2_OK_P1c, DDR2CTRLFPGA_2_OK_M1b, DDR2CTRLFPGA_2_OK_M2c, DDR2CTRLFPGA_2_RESET, DDR2CTRLFPGA_2_C8b-7, DDR2CTRLFPGA_2_DQS0-8.

DDR2_CTRLFPGA_4

Table of DDR2_CTRLFPGA_4 signals including DDR2CTRLFPGA_4_DQ0-15, DDR2CTRLFPGA_4_DM0-3, DDR2CTRLFPGA_4_A0-13, DDR2CTRLFPGA_4_BA0-1, DDR2CTRLFPGA_4_WE, DDR2CTRLFPGA_4_TAS, DDR2CTRLFPGA_4_CAS, DDR2CTRLFPGA_4_S_0b, DDR2CTRLFPGA_4_S_1c, DDR2CTRLFPGA_4_ODT0b, DDR2CTRLFPGA_4_ODT1c, DDR2CTRLFPGA_4_CKE, DDR2CTRLFPGA_4_KE, DDR2CTRLFPGA_4_OK_P0b, DDR2CTRLFPGA_4_OK_P1c, DDR2CTRLFPGA_4_OK_M1b, DDR2CTRLFPGA_4_OK_M2c, DDR2CTRLFPGA_4_RESET, DDR2CTRLFPGA_4_C8b-7, DDR2CTRLFPGA_4_DQS0-8.

DDR2_FPGA_2

Table of DDR2_FPGA_2 signals including DDR2FPGA2_DQ0-15, DDR2FPGA2_DM0-3, DDR2FPGA2_A0-13, DDR2FPGA2_BA0-1, DDR2FPGA2_WE, DDR2FPGA2_TAS, DDR2FPGA2_CAS, DDR2FPGA2_S_0b, DDR2FPGA2_S_1c, DDR2FPGA2_ODT0b, DDR2FPGA2_ODT1c, DDR2FPGA2_CKE, DDR2FPGA2_KE, DDR2FPGA2_OK_P0b, DDR2FPGA2_OK_P1c, DDR2FPGA2_OK_M1b, DDR2FPGA2_OK_M2c, DDR2FPGA2_RESET, DDR2FPGA2_C8b-7, DDR2FPGA2_DQS0-8.

DDR2_FPGA_4

Table of DDR2_FPGA_4 signals including DDR2FPGA4_DQ0-15, DDR2FPGA4_DM0-3, DDR2FPGA4_A0-13, DDR2FPGA4_BA0-1, DDR2FPGA4_WE, DDR2FPGA4_TAS, DDR2FPGA4_CAS, DDR2FPGA4_S_0b, DDR2FPGA4_S_1c, DDR2FPGA4_ODT0b, DDR2FPGA4_ODT1c, DDR2FPGA4_CKE, DDR2FPGA4_KE, DDR2FPGA4_OK_P0b, DDR2FPGA4_OK_P1c, DDR2FPGA4_OK_M1b, DDR2FPGA4_OK_M2c, DDR2FPGA4_RESET, DDR2FPGA4_C8b-7, DDR2FPGA4_DQS0-8.

DDR2_FPGA2_1

Table of DDR2_FPGA2_1 pin connections, including signals like DDR2FPGA2_1_DQ0-15, DDR2FPGA2_1_DM0-3, and DDR2FPGA2_1_DQS0-3.

DDR2_FPGA2_3

Table of DDR2_FPGA2_3 pin connections, including signals like DDR2FPGA2_3_DQ0-15, DDR2FPGA2_3_DM0-3, and DDR2FPGA2_3_DQS0-3.

DDR2_FPGA3_1

Table of DDR2_FPGA3_1 pin connections, including signals like DDR2FPGA3_1_DQ0-15, DDR2FPGA3_1_DM0-3, and DDR2FPGA3_1_DQS0-3.

DDR2_FPGA3_3

Table of DDR2_FPGA3_3 pin connections, including signals like DDR2FPGA3_3_DQ0-15, DDR2FPGA3_3_DM0-3, and DDR2FPGA3_3_DQS0-3.

DDR2_FPGA2_2

Table of DDR2_FPGA2_2 pin connections, including signals like DDR2FPGA2_2_DQ0-15, DDR2FPGA2_2_DM0-3, and DDR2FPGA2_2_DQS0-3.

DDR2_FPGA2_4

Table of DDR2_FPGA2_4 pin connections, including signals like DDR2FPGA2_4_DQ0-15, DDR2FPGA2_4_DM0-3, and DDR2FPGA2_4_DQS0-3.

DDR2_FPGA3_2

Table of DDR2_FPGA3_2 pin connections, including signals like DDR2FPGA3_2_DQ0-15, DDR2FPGA3_2_DM0-3, and DDR2FPGA3_2_DQS0-3.

DDR2_FPGA3_4

Table of DDR2_FPGA3_4 pin connections, including signals like DDR2FPGA3_4_DQ0-15, DDR2FPGA3_4_DM0-3, and DDR2FPGA3_4_DQS0-3.

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DDR2 MEMORY MODULES
DATA & CONTROL PORTS / PAGE 2

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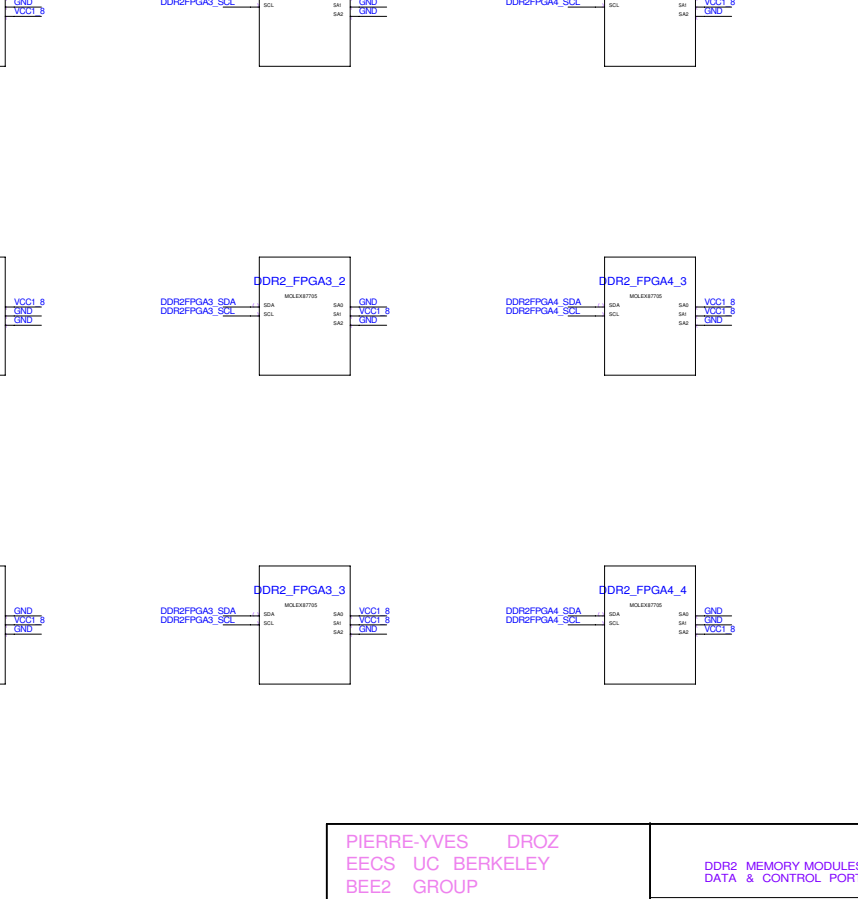
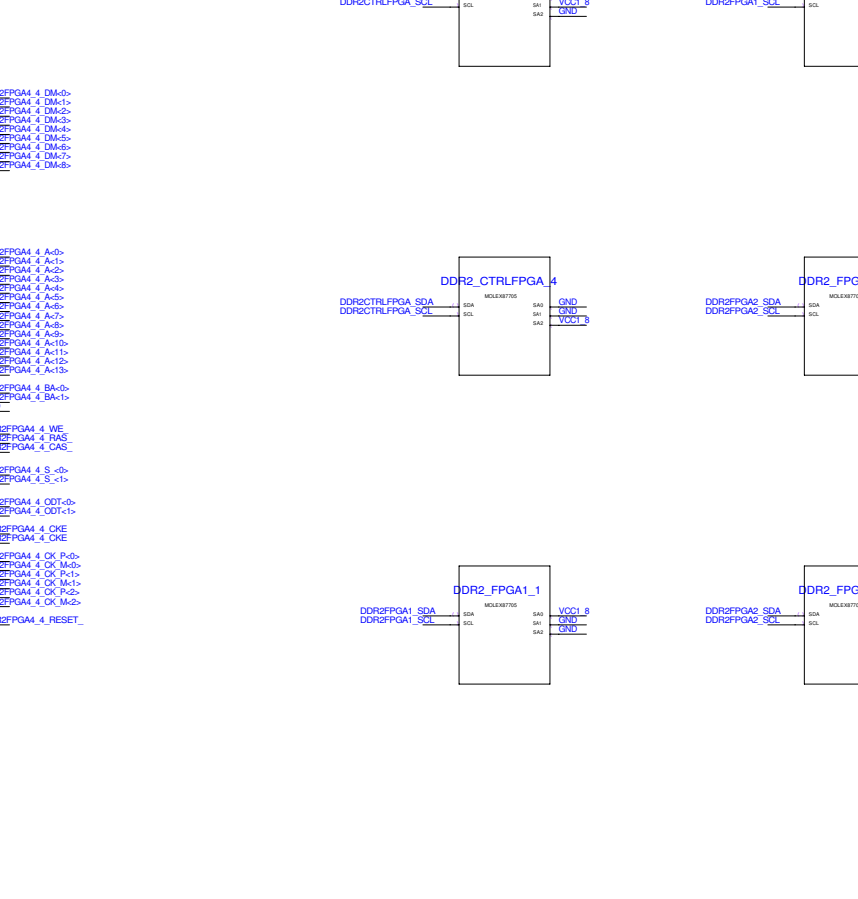
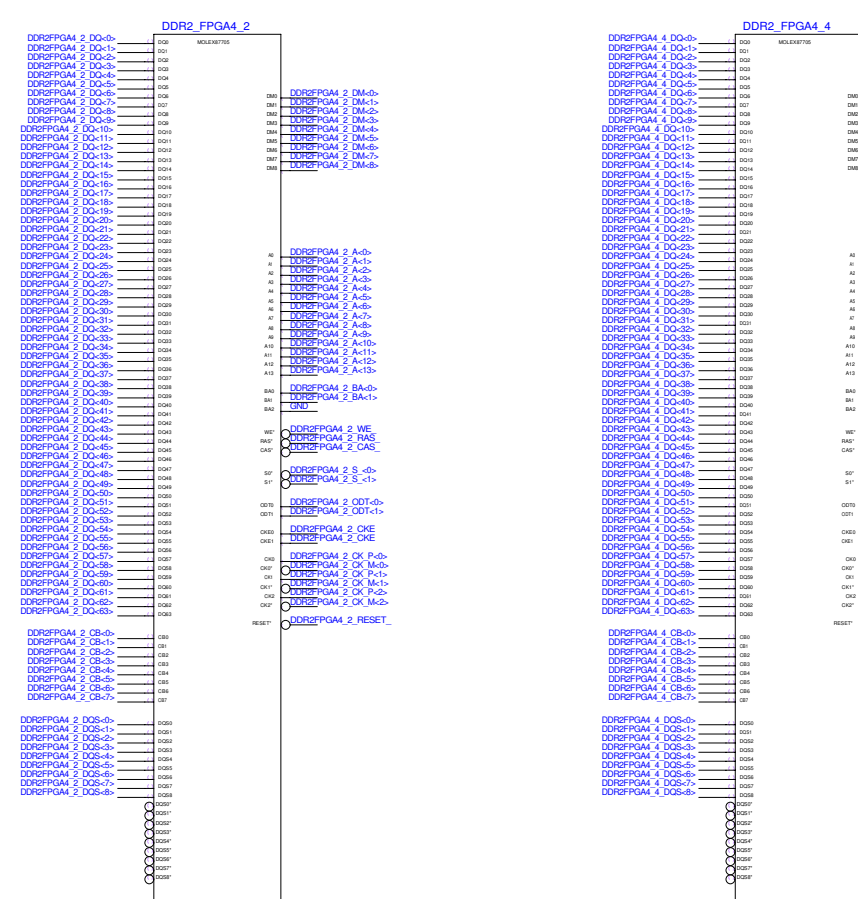
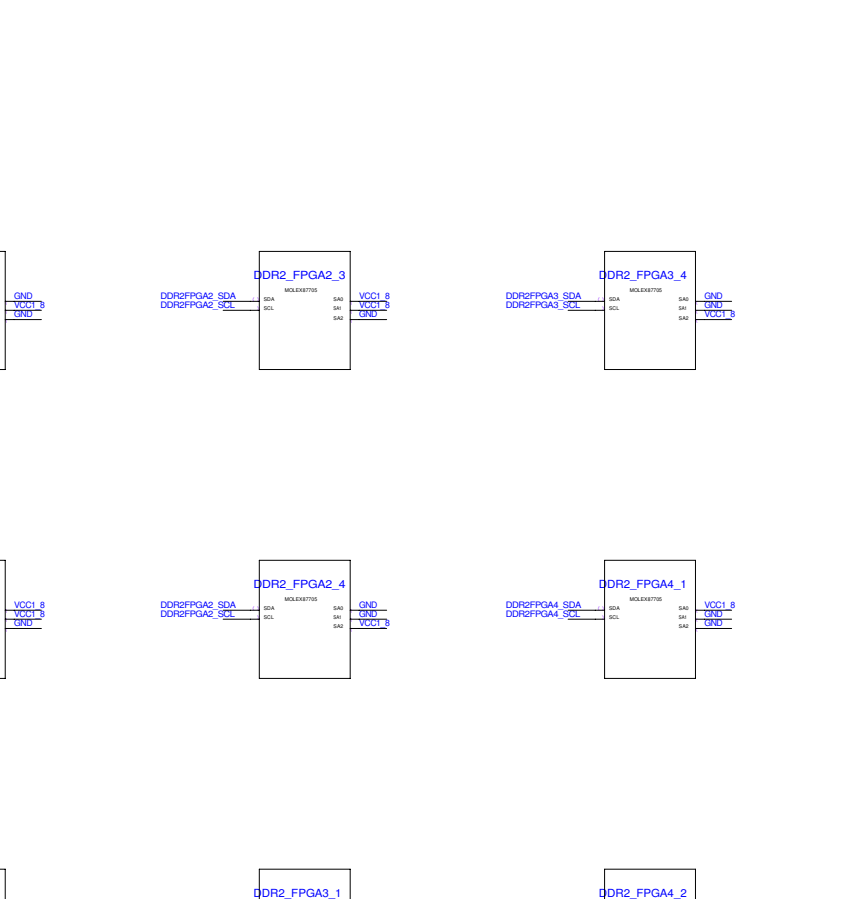
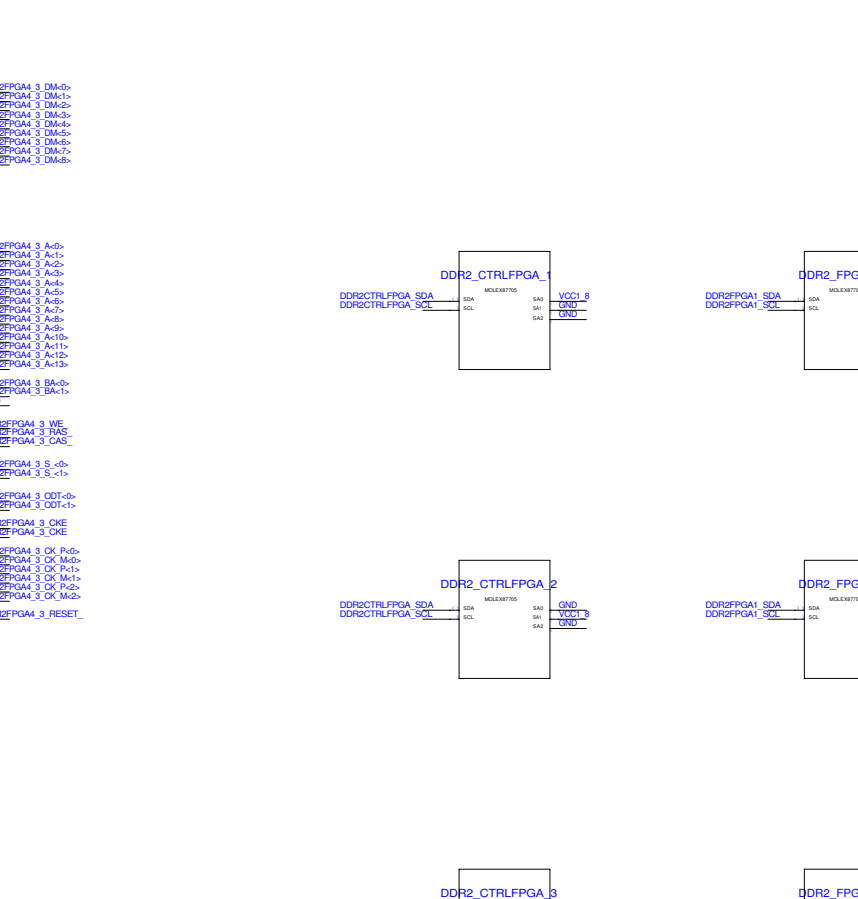
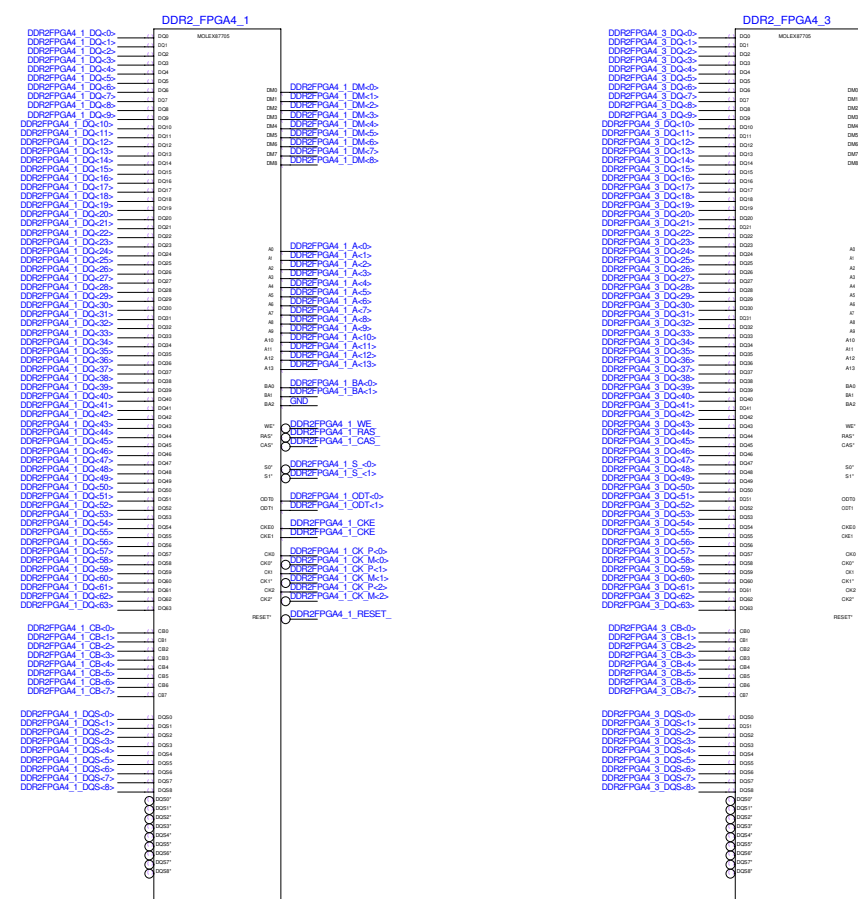
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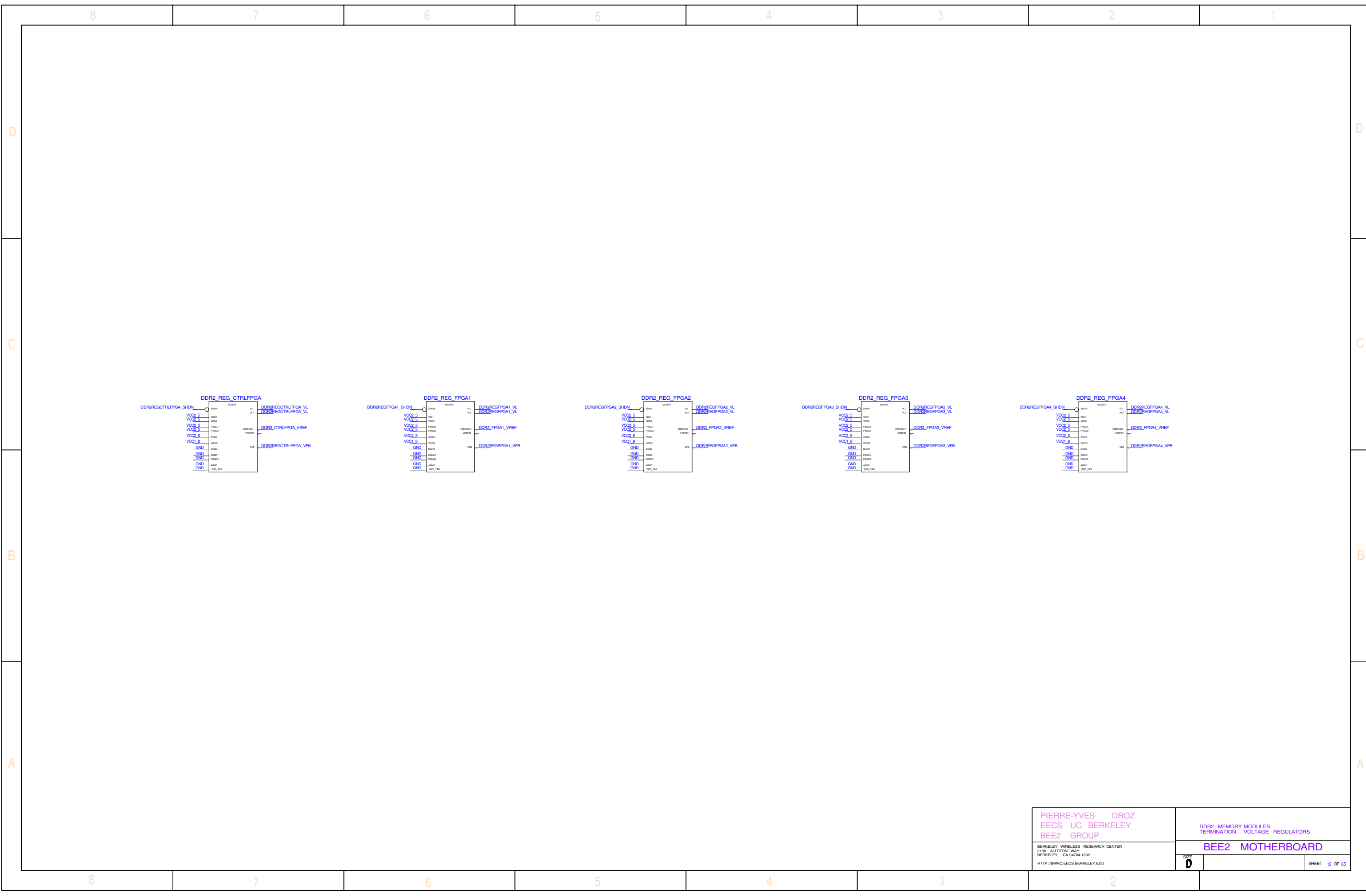
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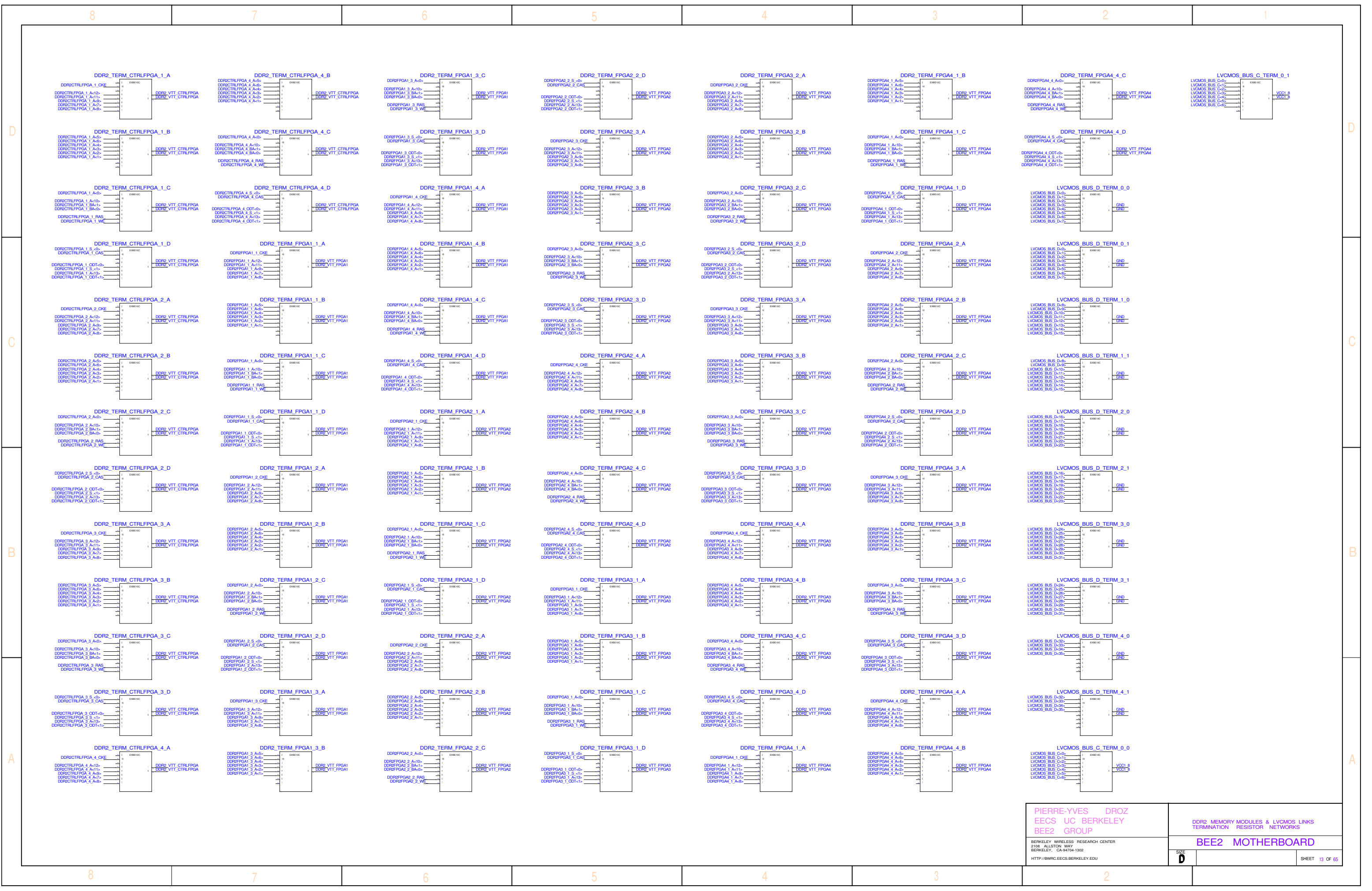
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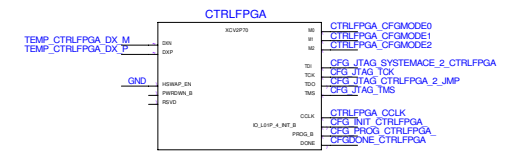
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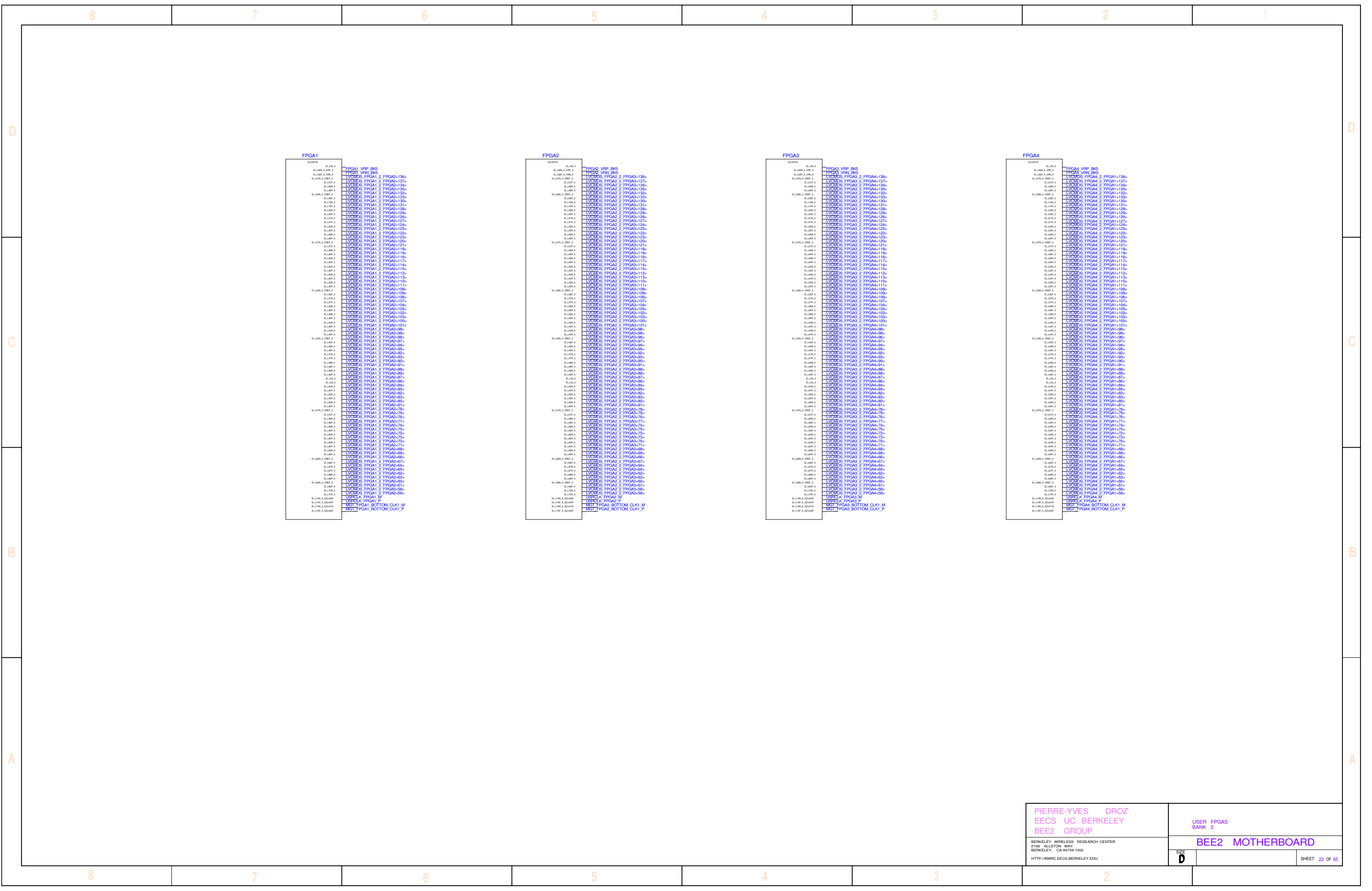






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HS_SATA_TOP_CTRLFPGA_1_RX_P	REF002	REF002	HS_SATA_BOTTOM_CTRLFPGA_9_RX_P
HS_SATA_TOP_CTRLFPGA_1_RX_M	REF002	REF002	HS_SATA_BOTTOM_CTRLFPGA_9_RX_M





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SIDE
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SHEET 23 OF 65

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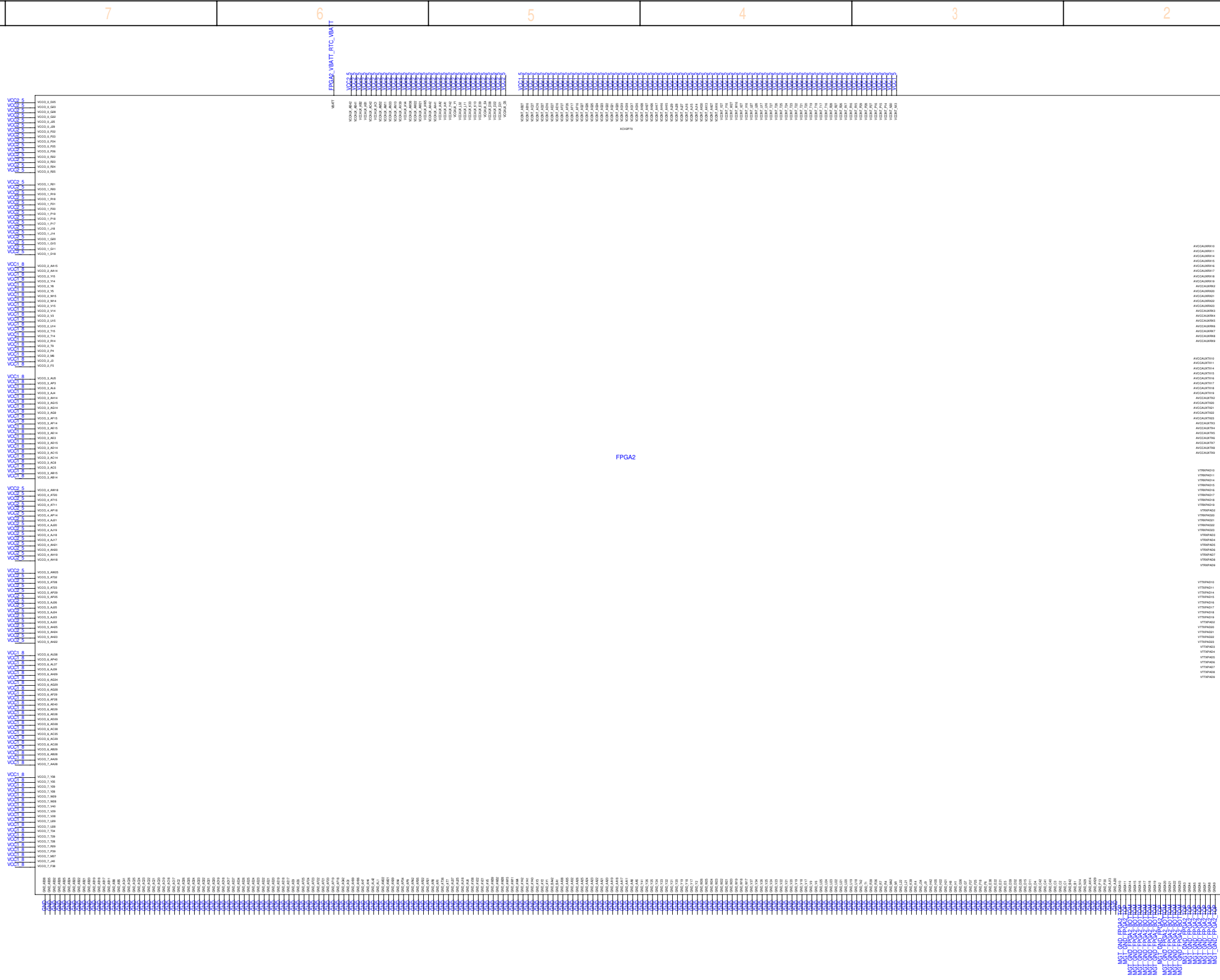
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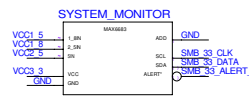
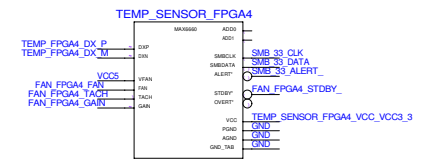
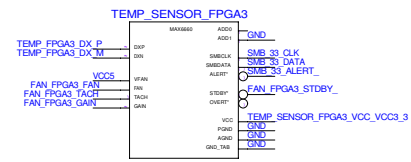
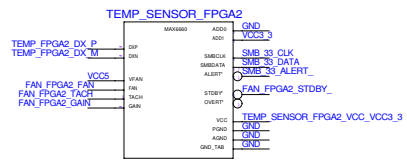
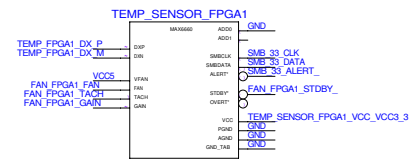
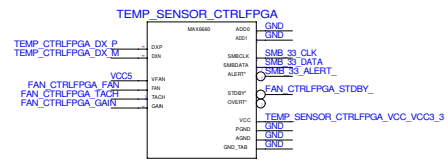
USER FPGAS
POWER / PAGE 2

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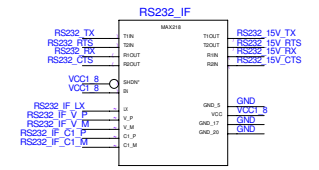
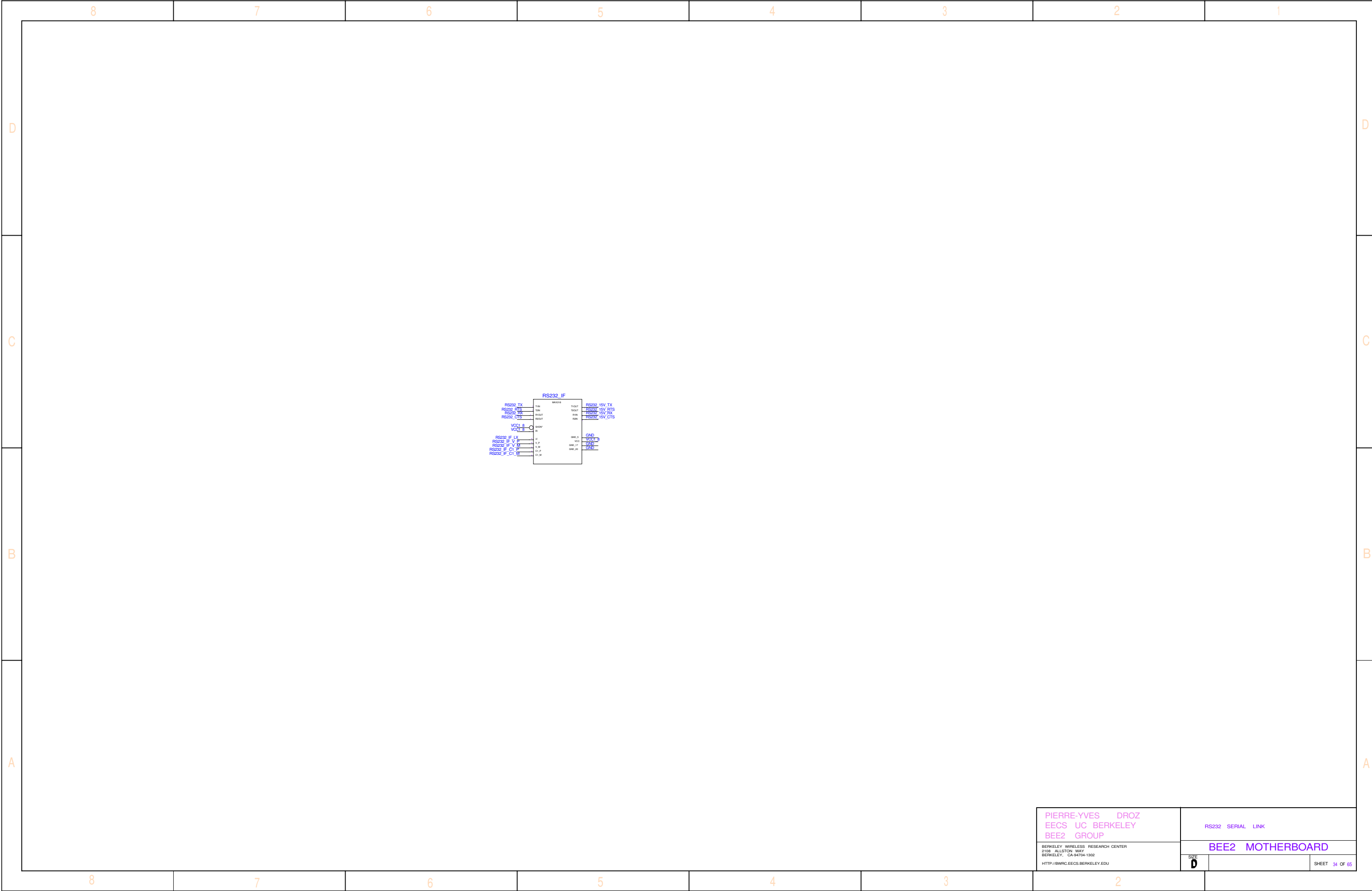


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REAL TIME CLOCK
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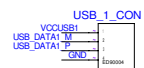
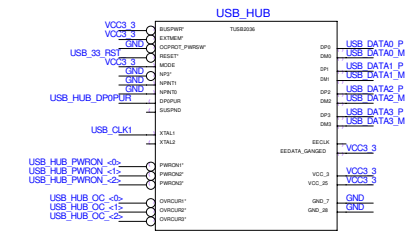
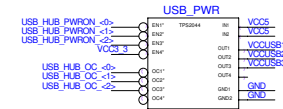
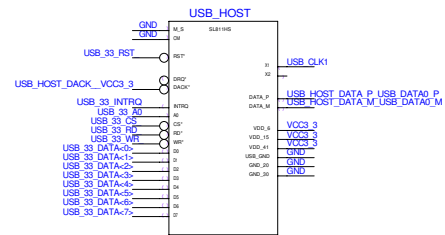
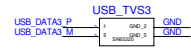
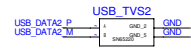
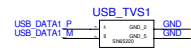
SIZE **D**
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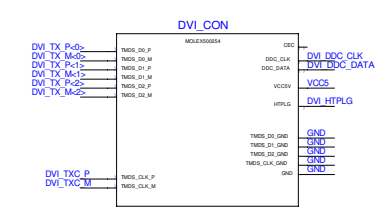
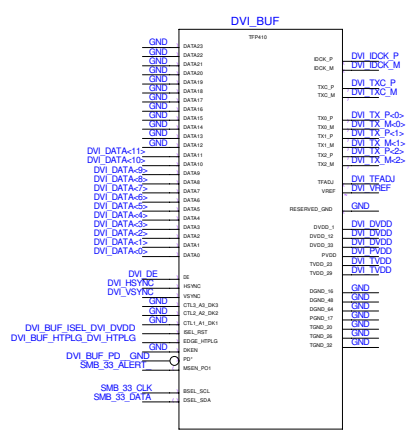
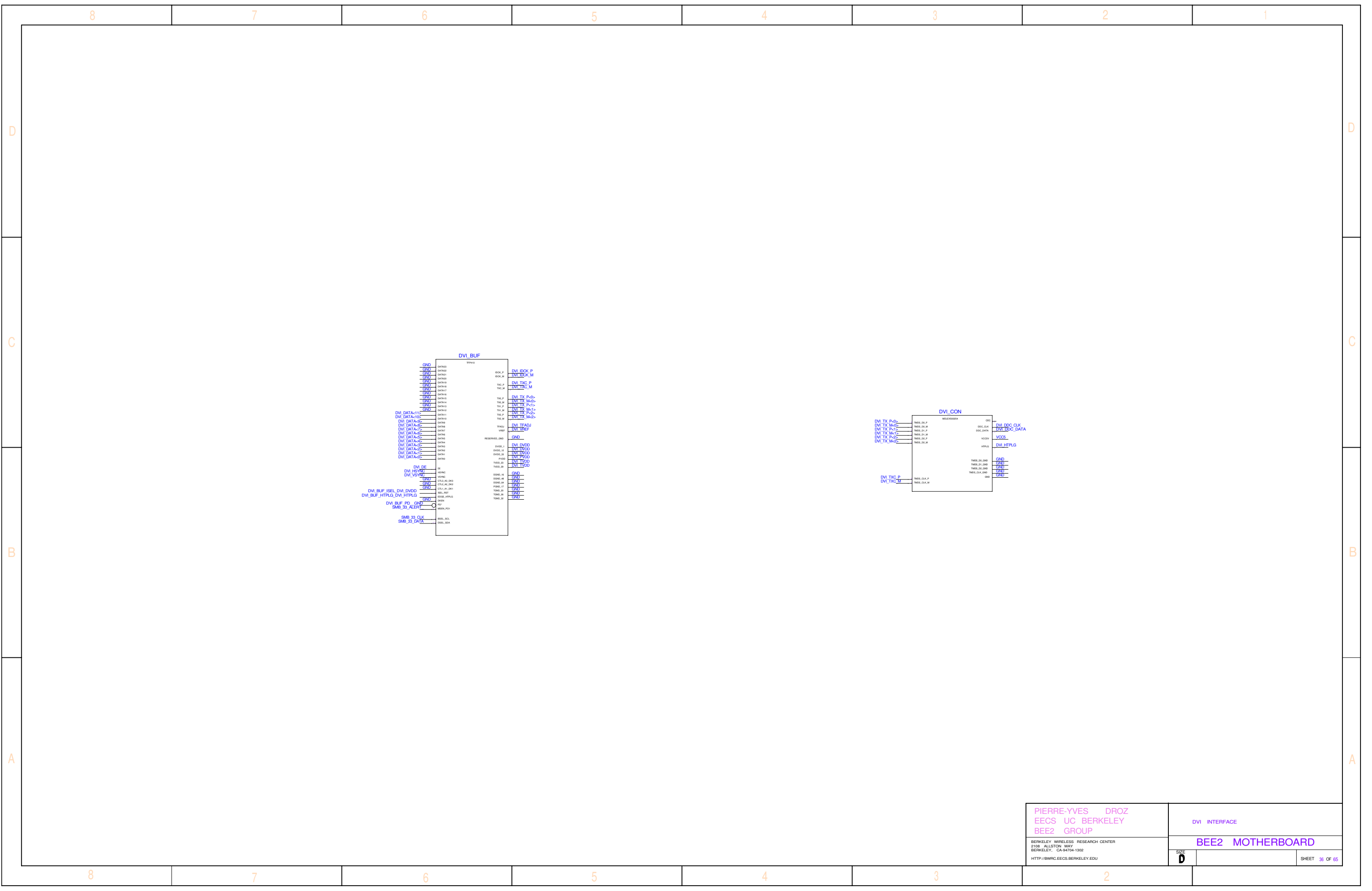
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BERKELEY WIRELESS RESEARCH CENTER 2108 ALLSTON WAY BERKELEY, CA 94704-1302 HTTP://BWRC.EECS.BERKELEY.EDU		BEE2 MOTHERBOARD	
SIZE D			SHEET 34 OF 65

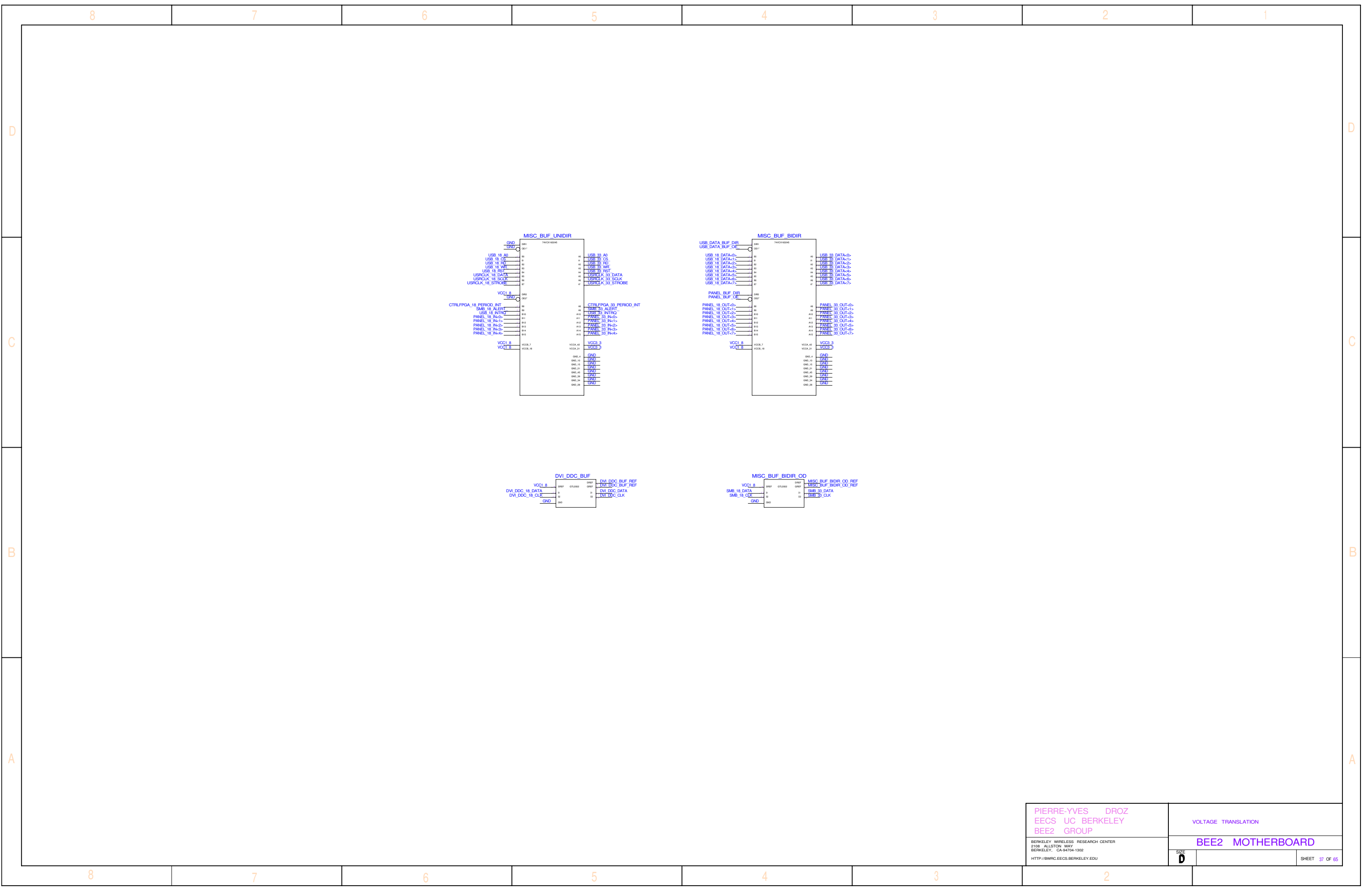
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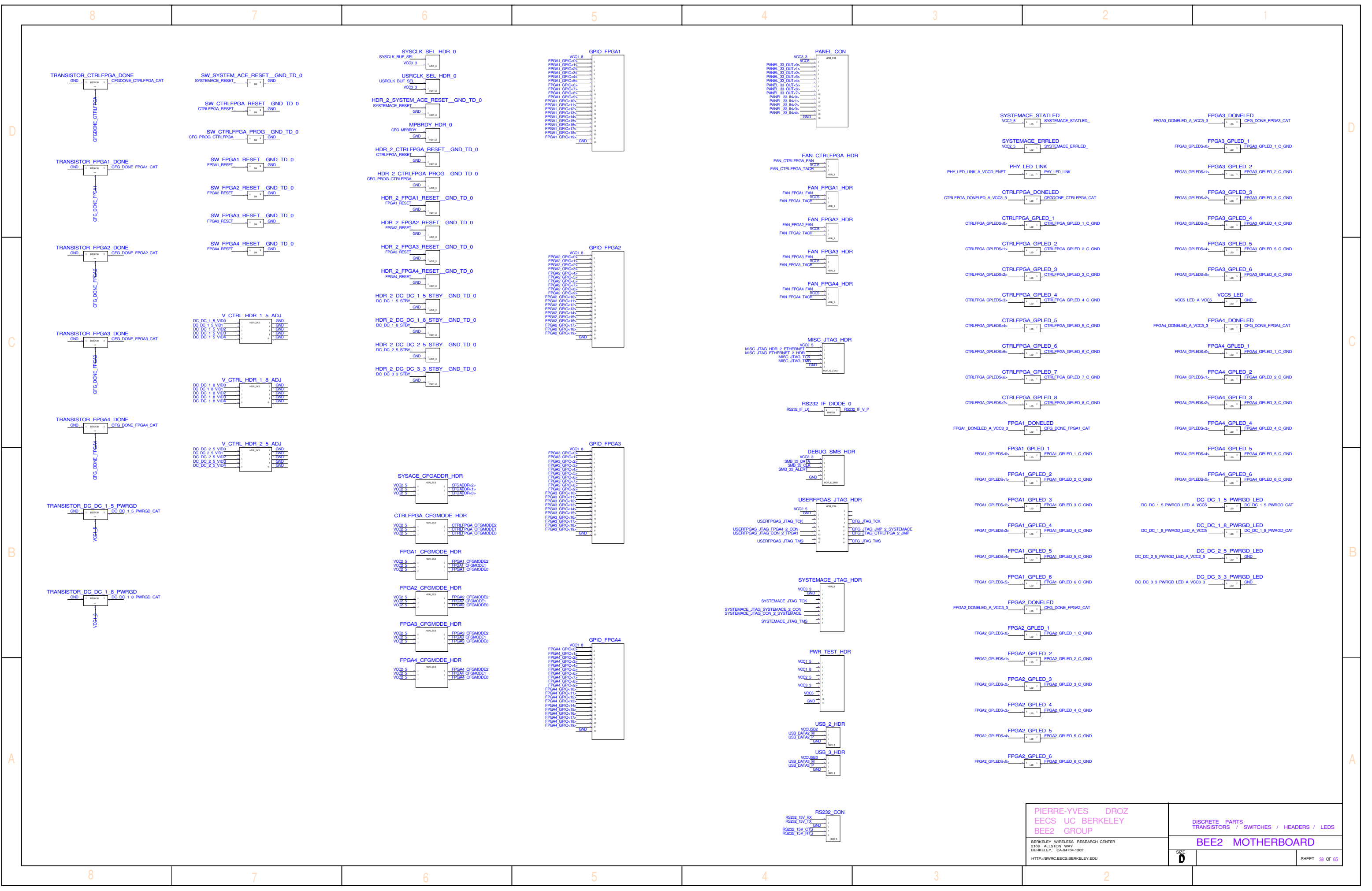
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PIERRE-YVES DROZ
 EECS UC BERKELEY
 BEE2 GROUP

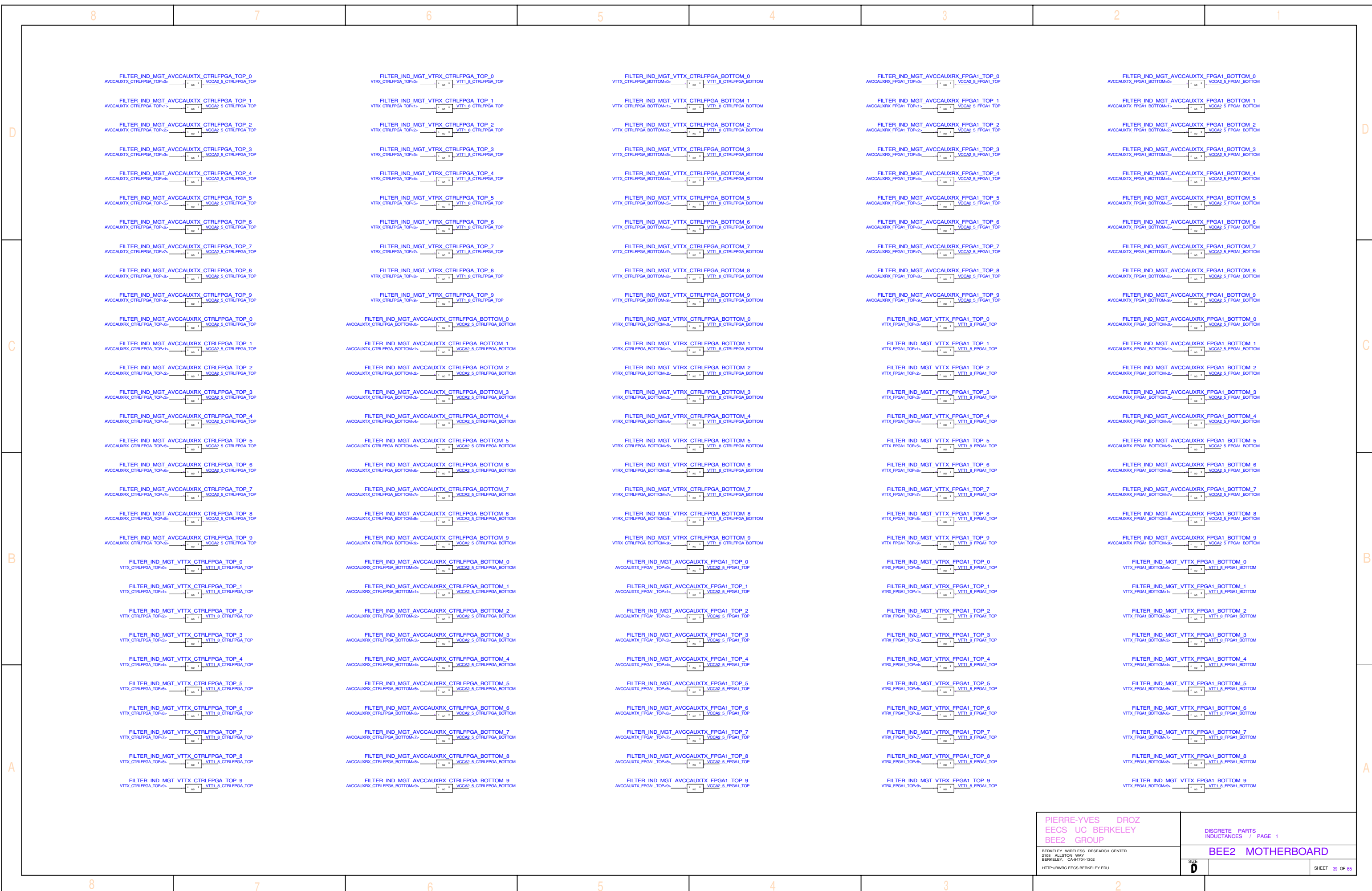
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 2108 ALLSTON WAY
 BERKELEY, CA 94704-1002
 HTTP://BWRC.EECS.BERKELEY.EDU

DISCRETE PARTS
 TRANSISTORS / SWITCHES / HEADERS / LEDS

BEE2 MOTHERBOARD

SIDE **D**

SHEET 38 OF 65



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EECS UC BERKELEY
BEE2 GROUP

DISCRETE PARTS
INDUCTANCES / PAGE 1

BEE2 MOTHERBOARD

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HTTP://BWRC.EECS.BERKELEY.EDU

SIDE
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SHEET 38 OF 65

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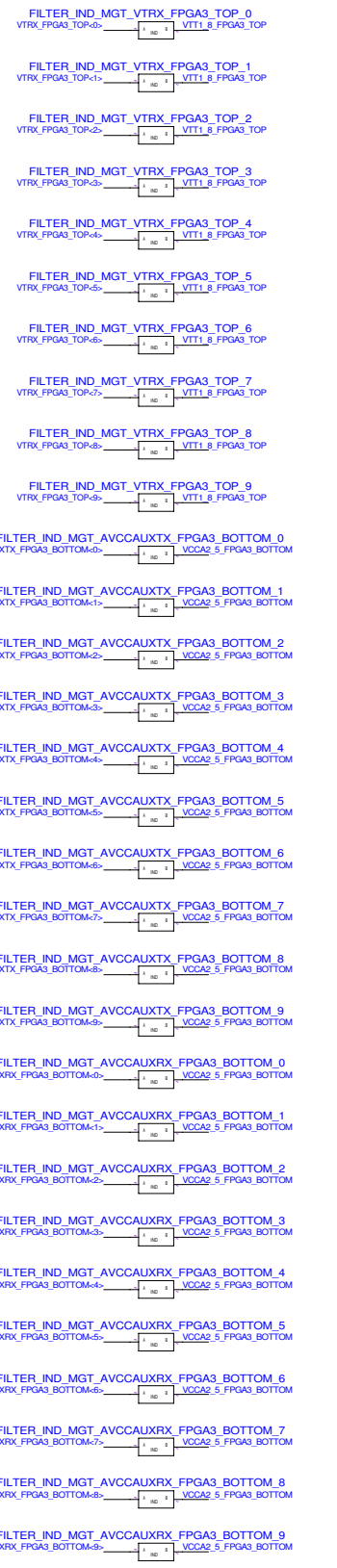
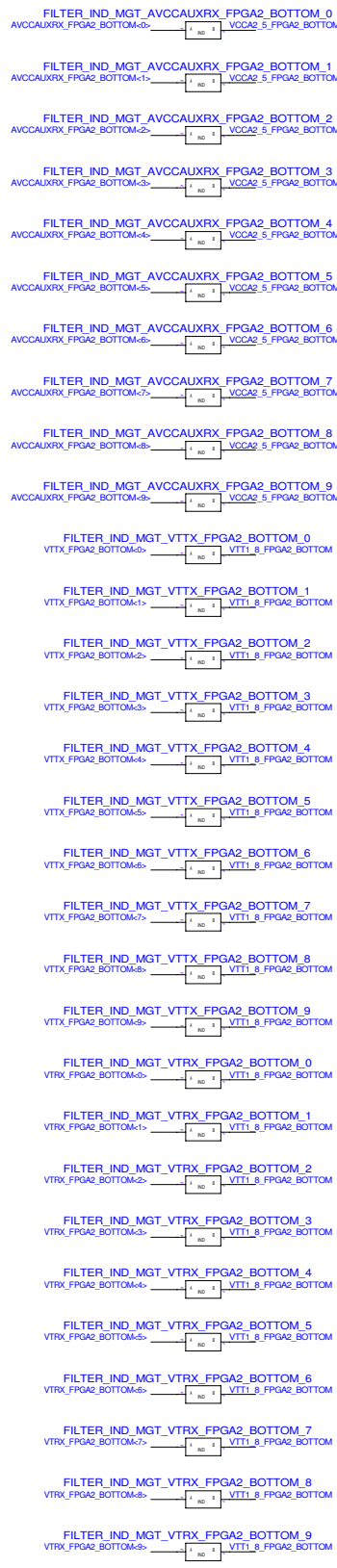
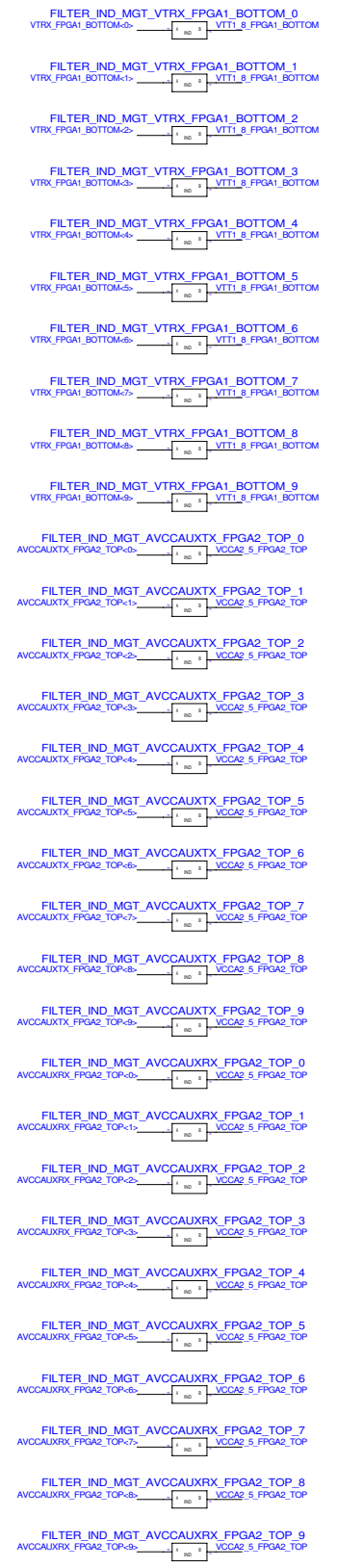
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PIERRE-YVES DROZ ECS UC BERKELEY BEE2 GROUP		DISCRETE PARTS INDUCTANCES / PAGE 2	
BERKELEY WIRELESS RESEARCH CENTER 2108 ALLSTON WAY BERKELEY, CA 94704-1302 HTTP://BWRC.ECS.BERKELEY.EDU		BEE2 MOTHERBOARD	
SIDE D		SHEET 40 OF 65	



PIERRE-YVES DROZ ECS UC BERKELEY BEE2 GROUP	DISCRETE PARTS INDUCTANCES / PAGE 3
BERKELEY WIRELESS RESEARCH CENTER 2108 ALLSTON WAY BERKELEY, CA 94704-1302 HTTP://BWRC.ECS.BERKELEY.EDU	BEE2 MOTHERBOARD
SIZE D	SHEET 41 OF 65

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PIERRE-YVES DROZ EECS UC BERKELEY BEE2 GROUP		DISCRETE PARTS RESISTORS / PAGE 1	
BERKELEY WIRELESS RESEARCH CENTER 2108 ALLSTON WAY BERKELEY, CA 94704-1002 HTTP://BWRC.EECS.BERKELEY.EDU		BEE2 MOTHERBOARD	
SIDE D		SHEET 42 OF 65	

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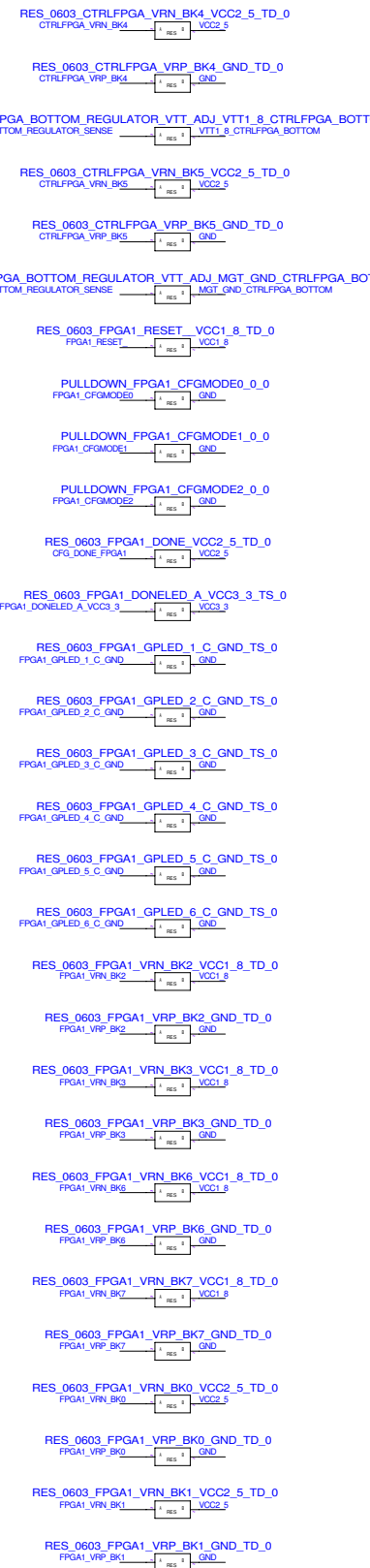
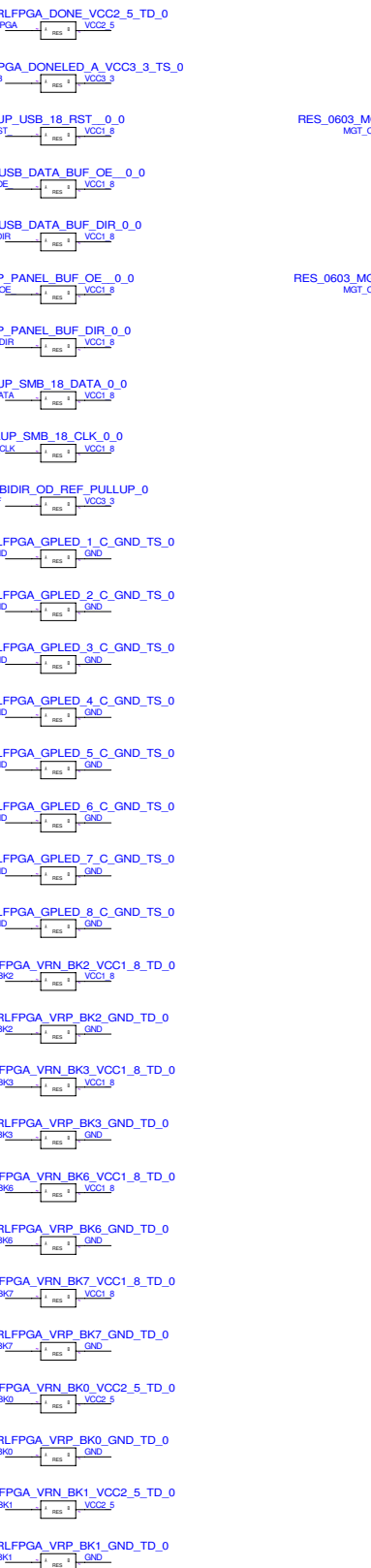
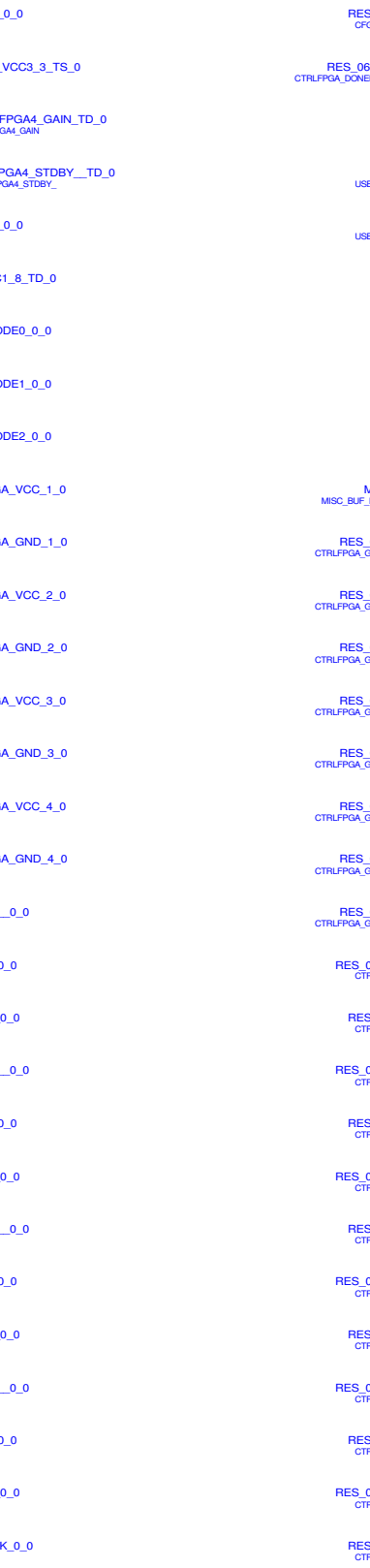
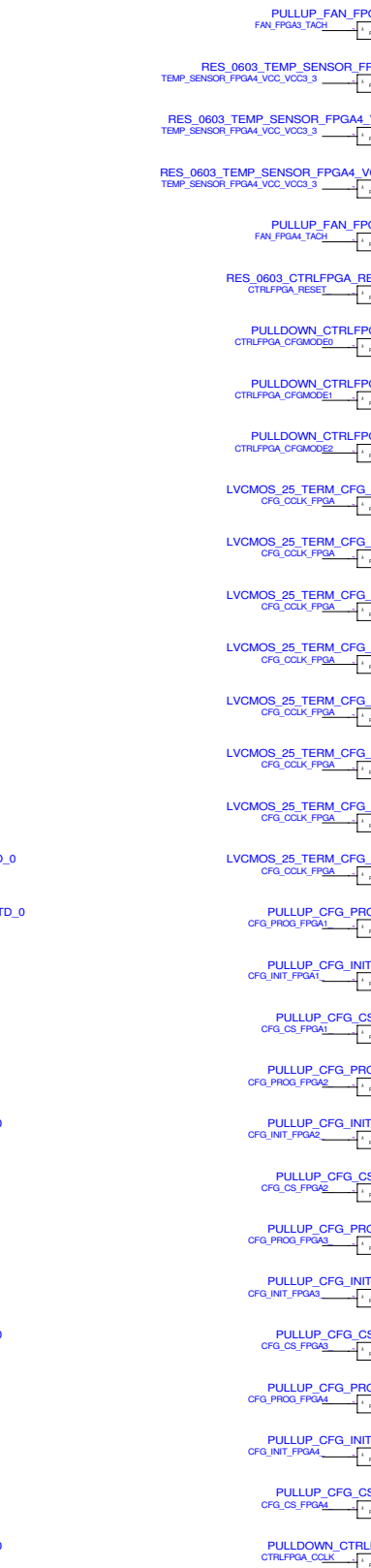
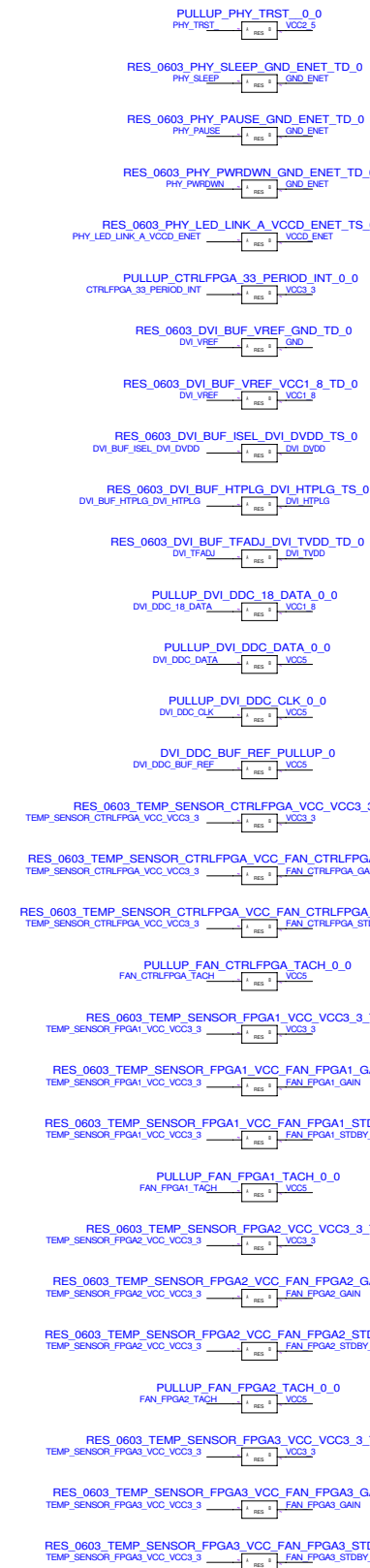
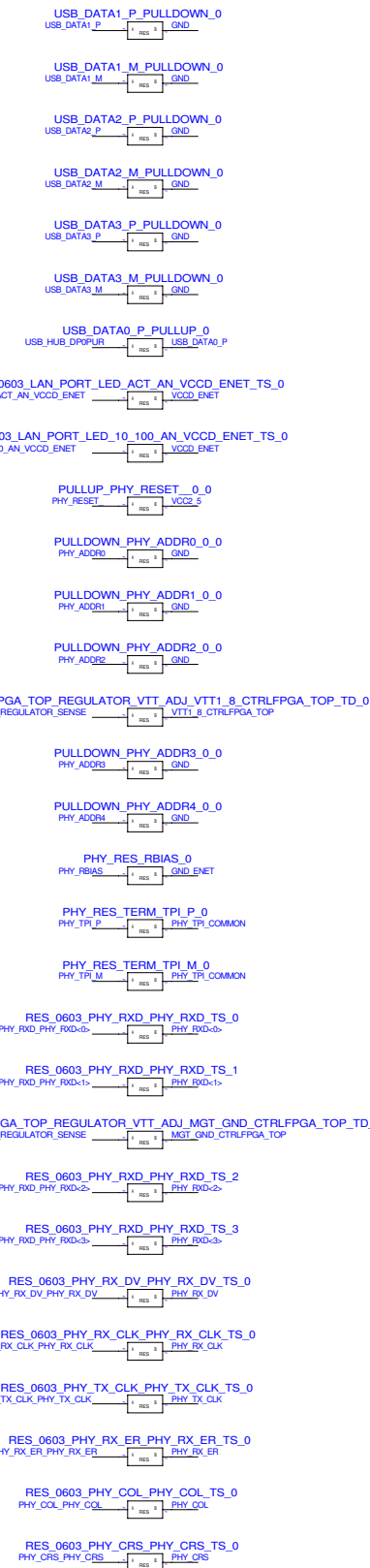
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PIERRE-YVES DROZ ECS UC BERKELEY BEE2 GROUP		DISCRETE PARTS RESISTORS / PAGE 3	
BERKELEY WIRELESS RESEARCH CENTER 2108 ALLSTON WAY BERKELEY, CA 94704-1302 HTTP://BWRC.ECS.BERKELEY.EDU		BEE2 MOTHERBOARD	
SIZE D		SHEET 44 OF 65	

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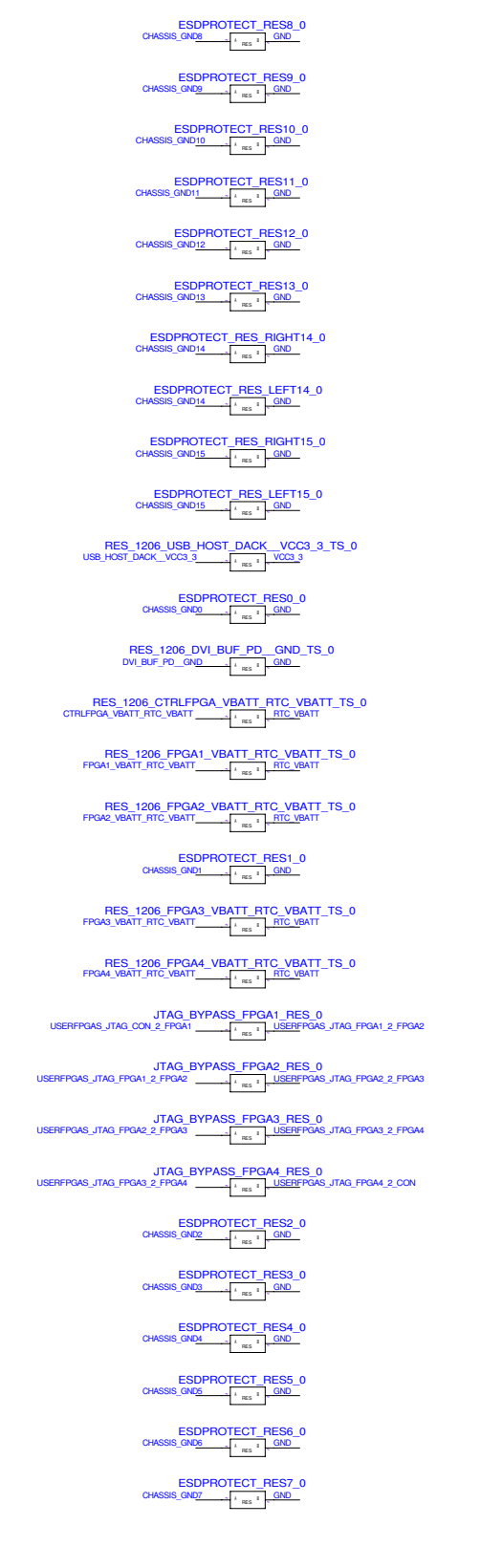
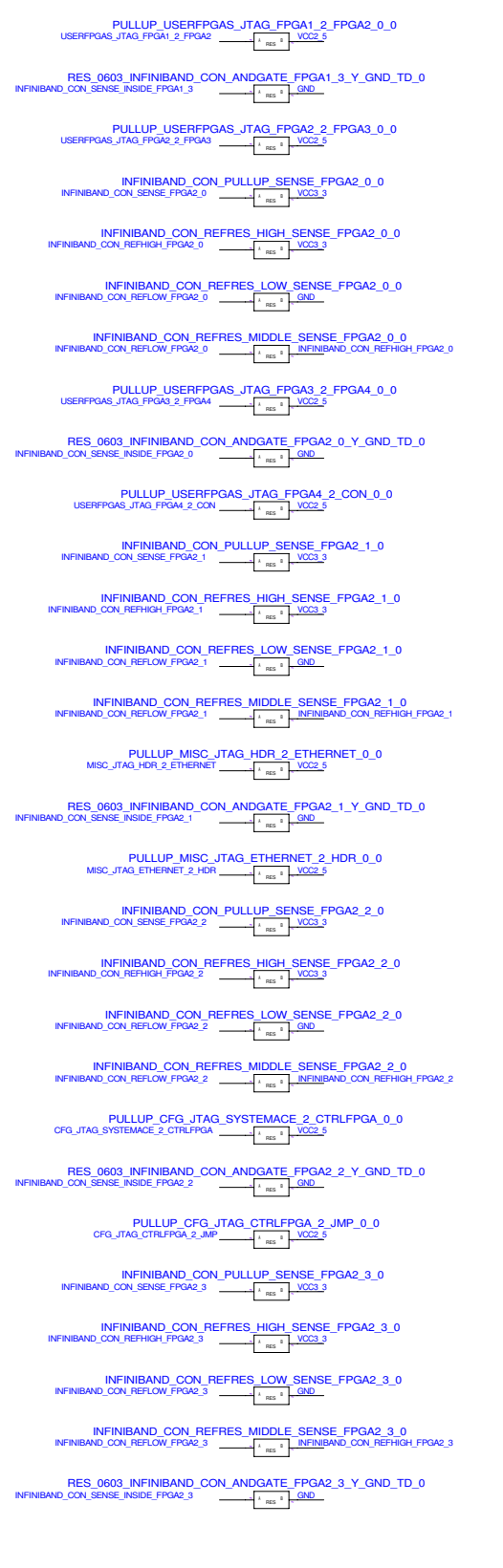
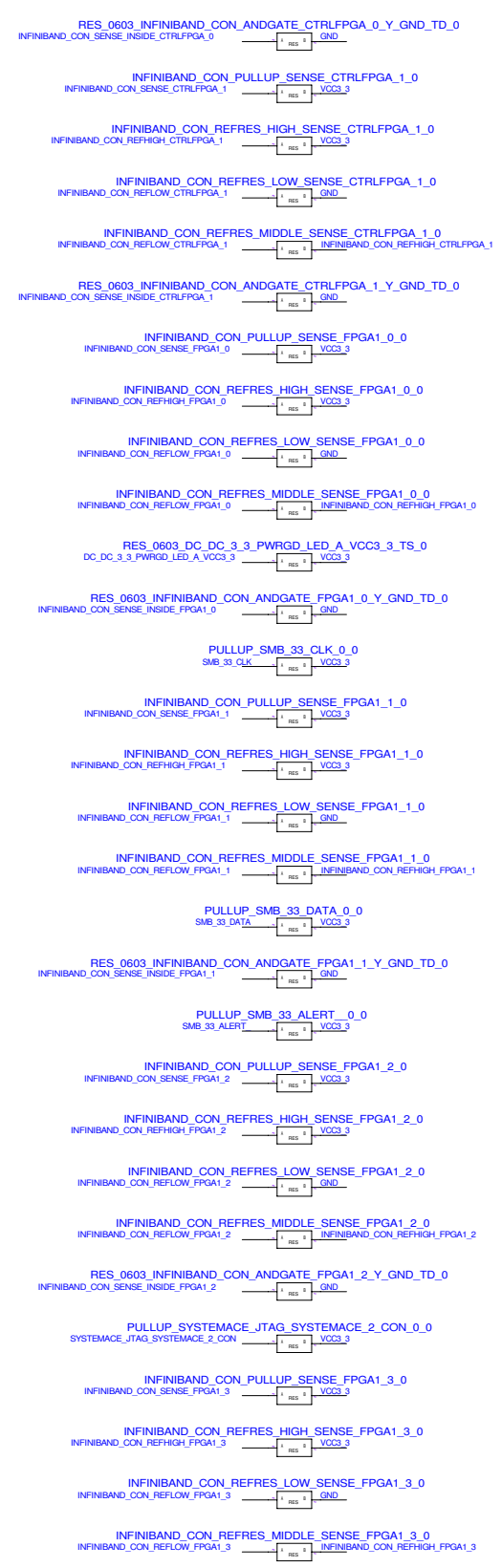
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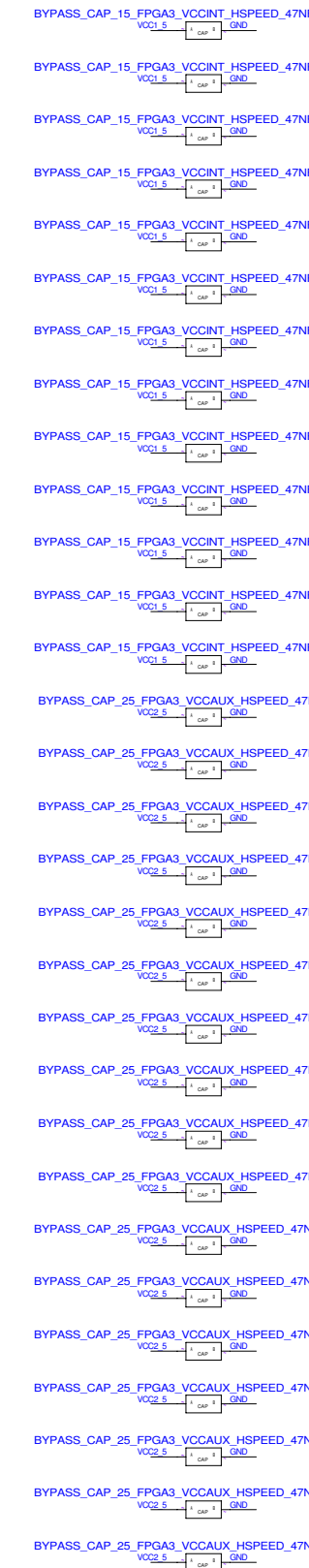
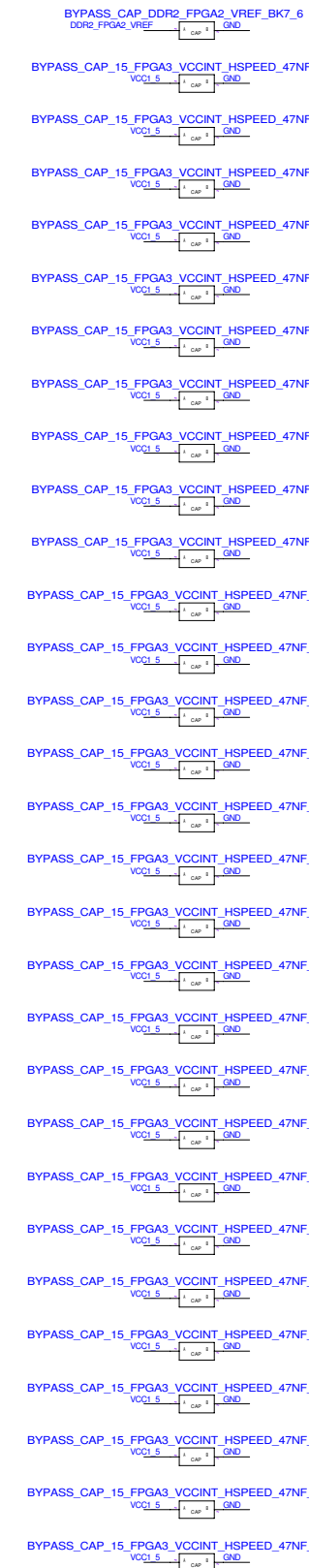
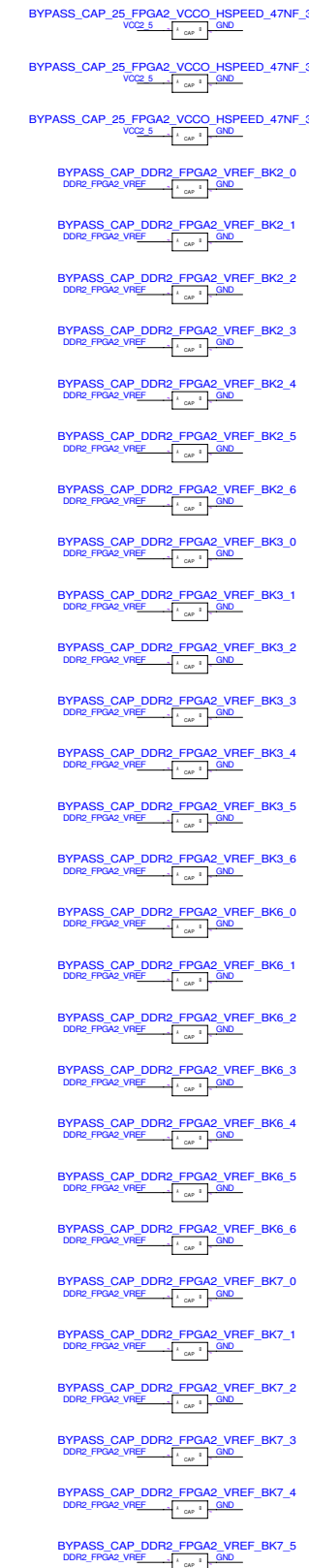
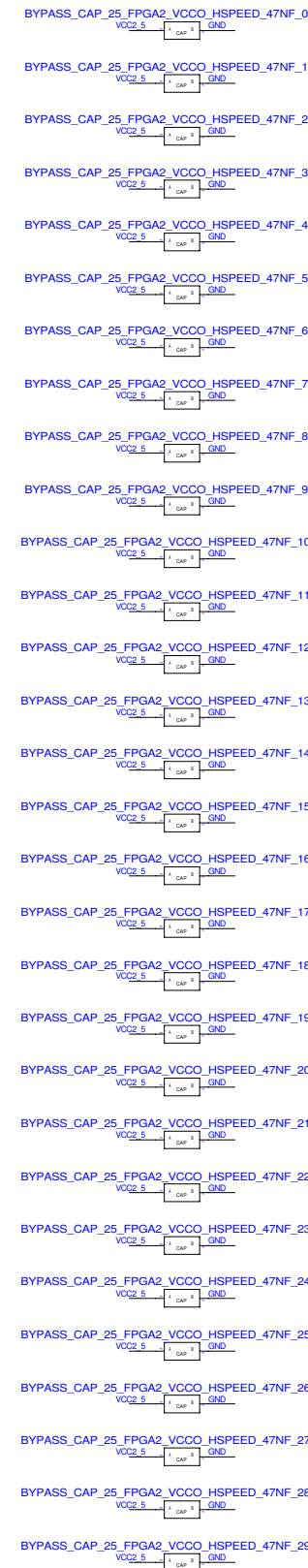
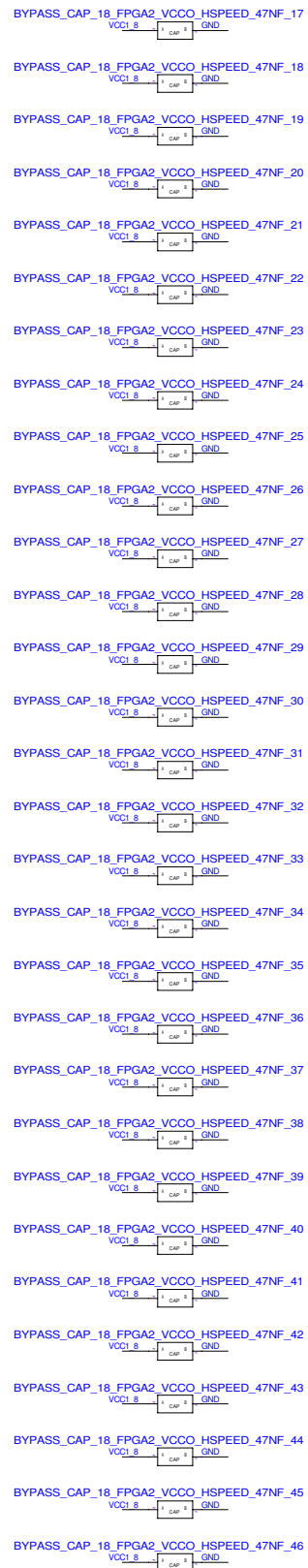
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PIERRE-YVES DROZ
 ECTS UC BERKELEY
 BEE2 GROUP

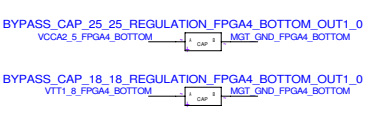
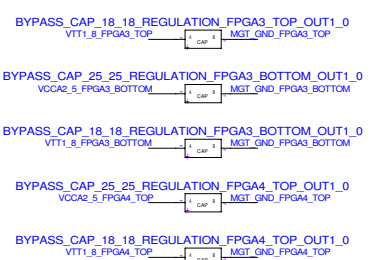
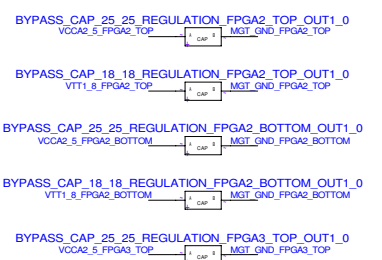
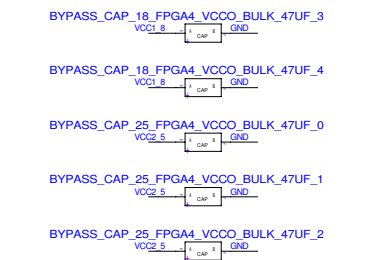
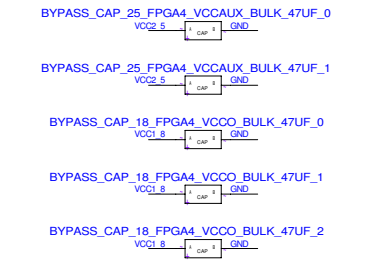
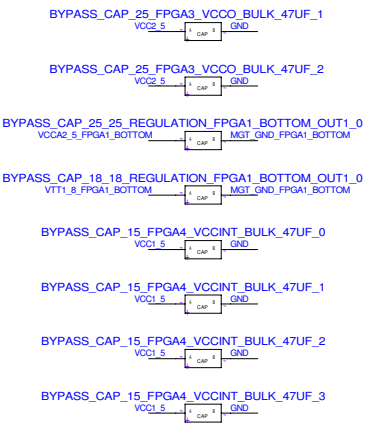
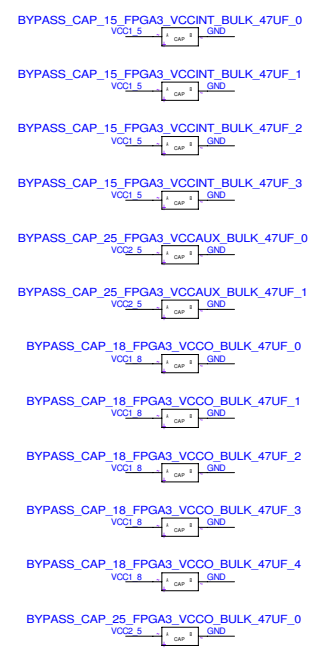
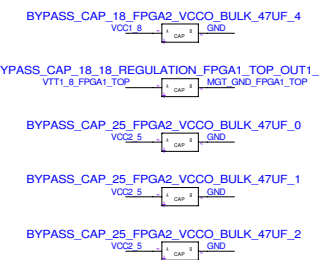
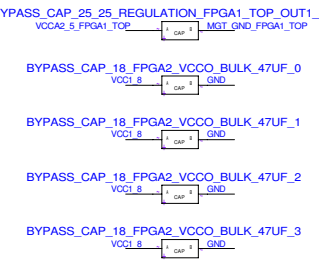
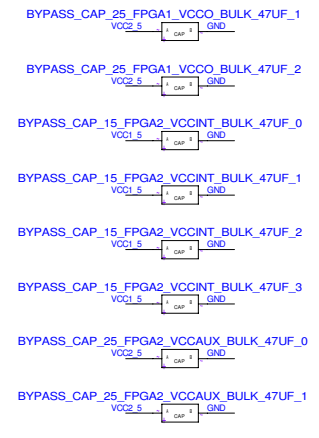
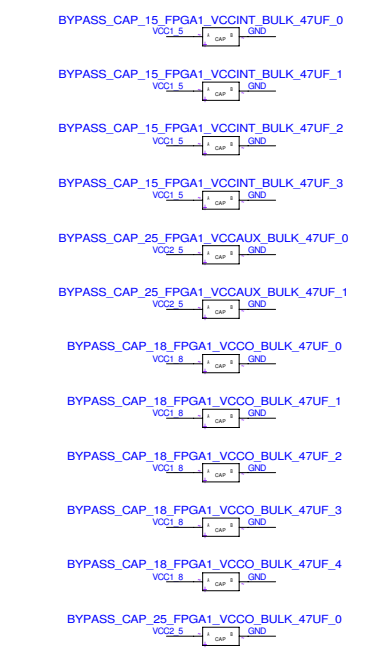
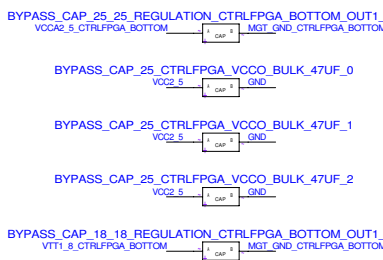
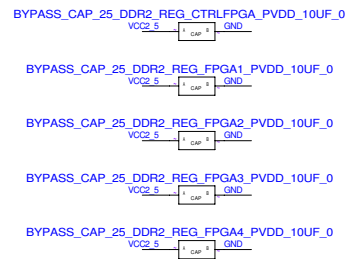
DISCRETE PARTS
 CAPACITORS / PAGE 11

BEE2 MOTHERBOARD

SIZE **D**

SHEET 56 OF 65

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BYPASS_CAP_25_FPGA3_VCCO_HSPEED_470NF_16
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PIERRE-YVES DROZ
EECS UC BERKELEY
BEE2 GROUP

DISCRETE PARTS
CAPACITORS / PAGE 15

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BEE2 MOTHERBOARD

SIZE
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SHEET 60 OF 65



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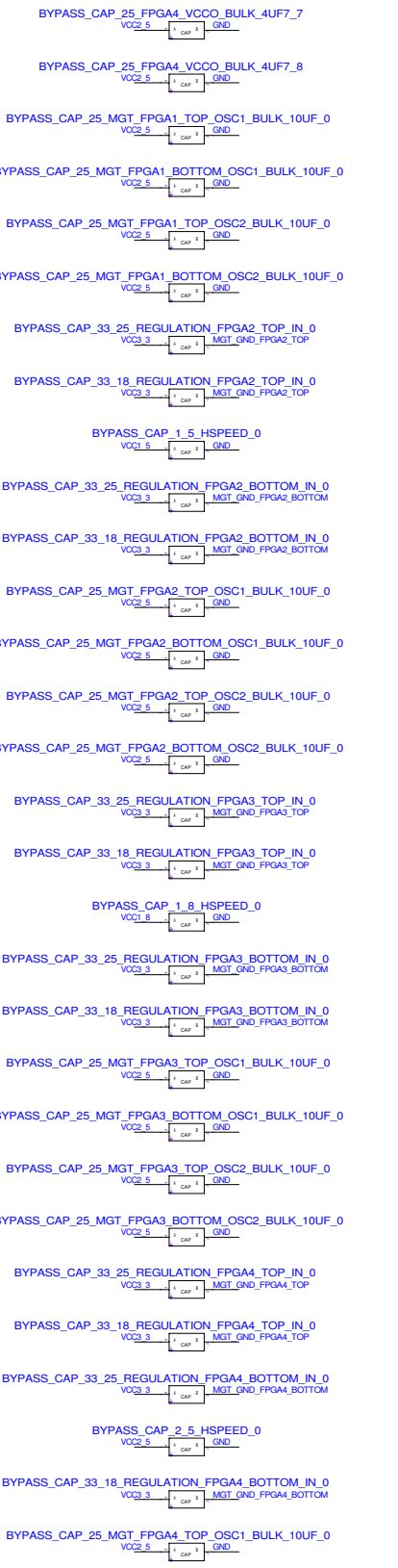
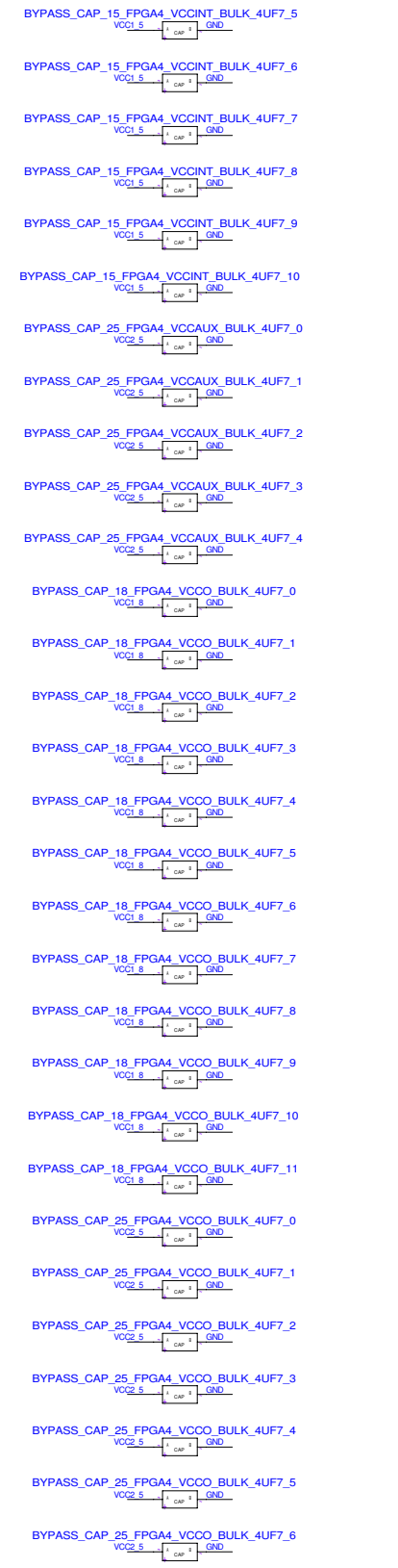
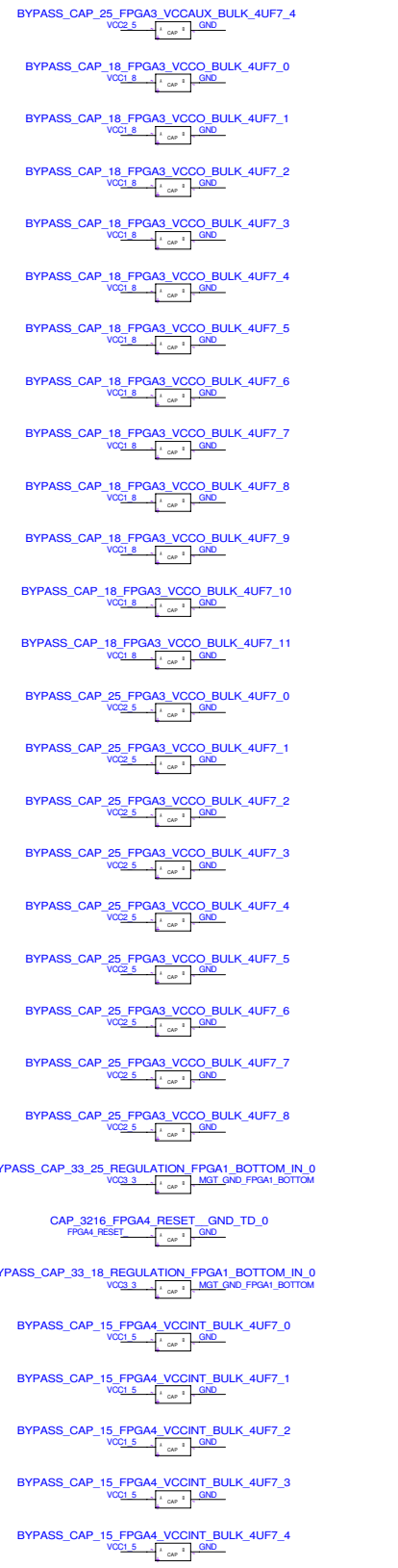
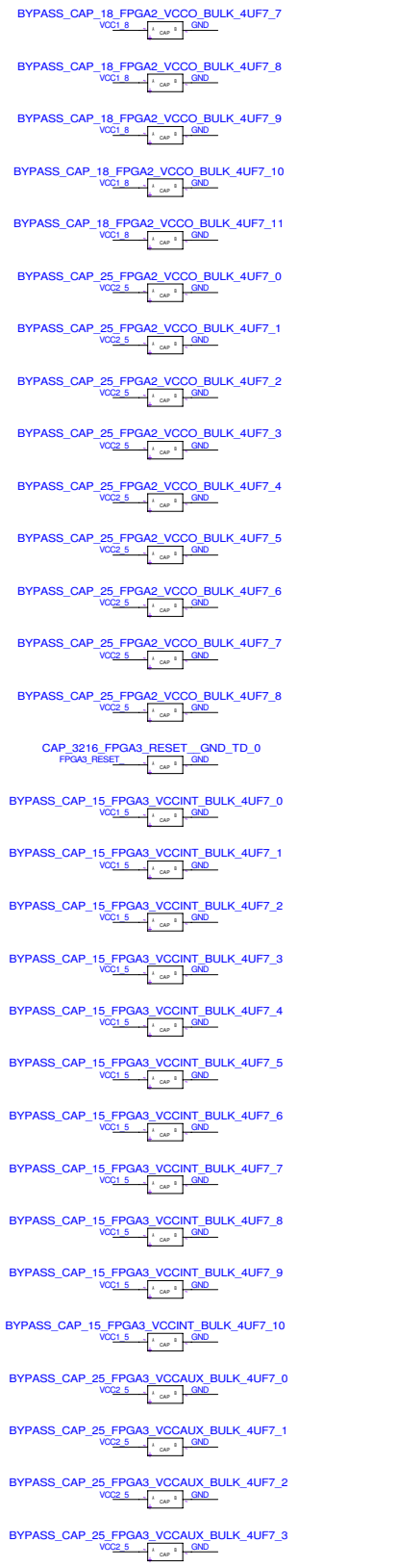
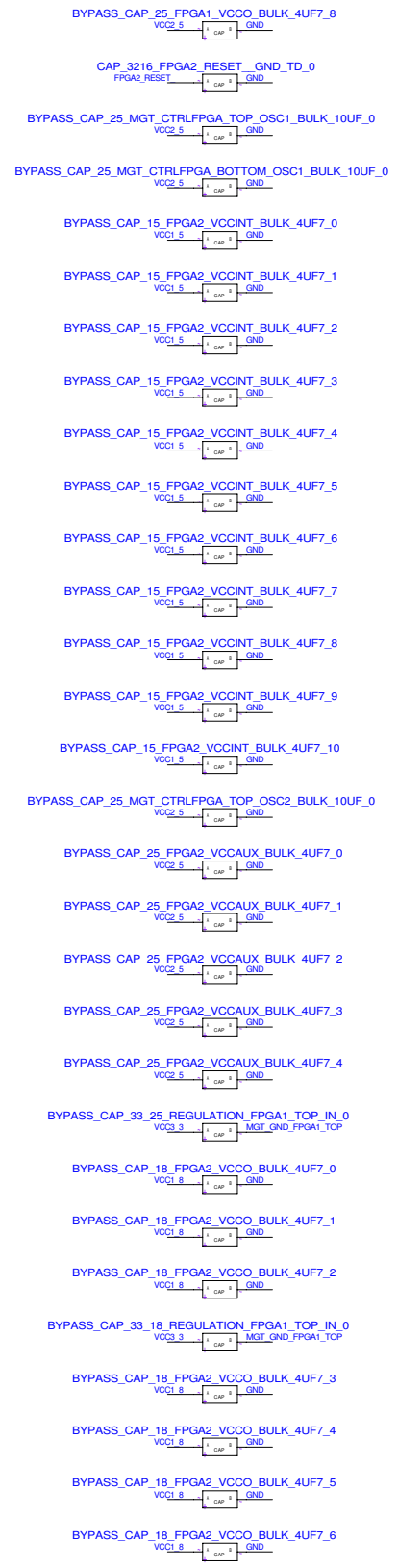
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PIERRE-YVES DROZ ECS UC BERKELEY BEE2 GROUP		DISCRETE PARTS CAPACITORS / PAGE 17	
BERKELEY WIRELESS RESEARCH CENTER 2108 ALLSTON WAY BERKELEY, CA 94704-1002 HTTP://BWRC.ECS.BERKELEY.EDU		BEE2 MOTHERBOARD	
SIDE D		SHEET 62 OF 65	

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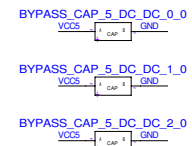
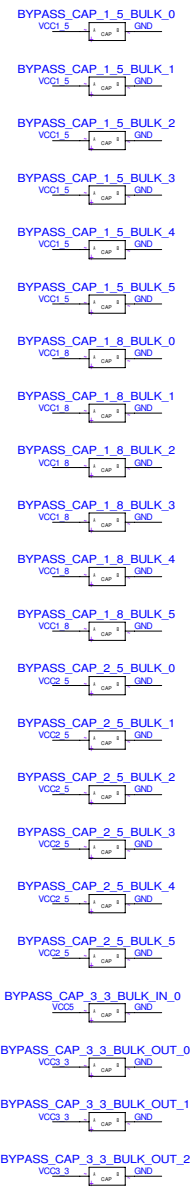
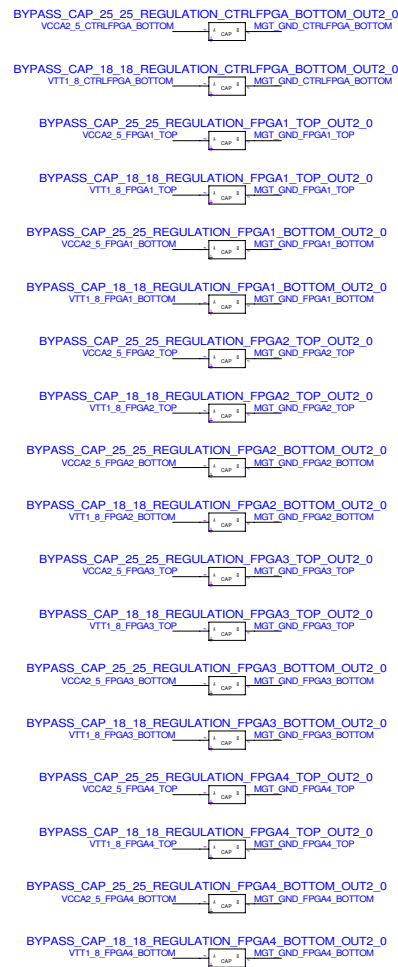
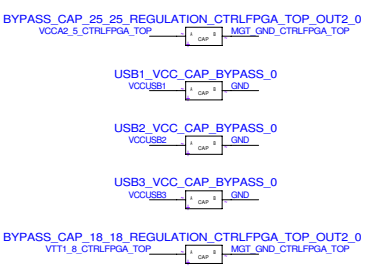
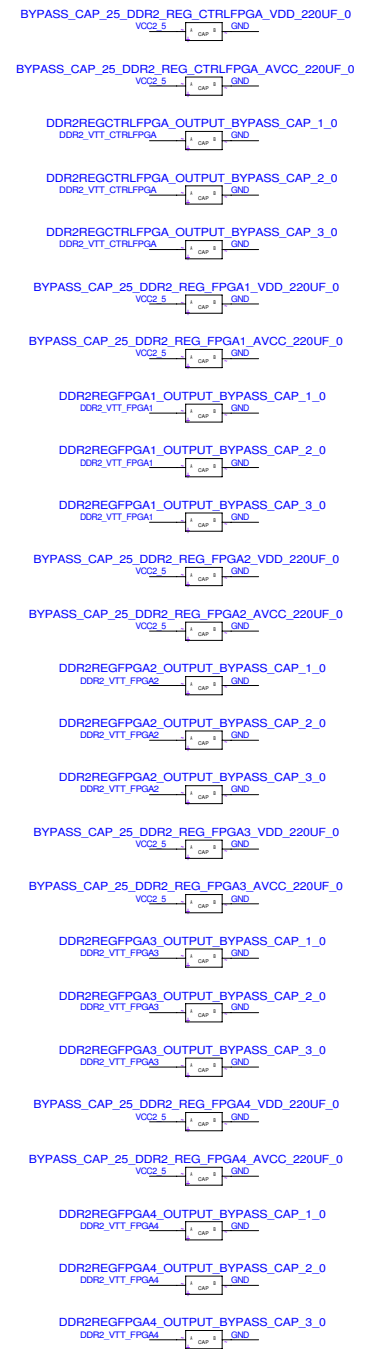
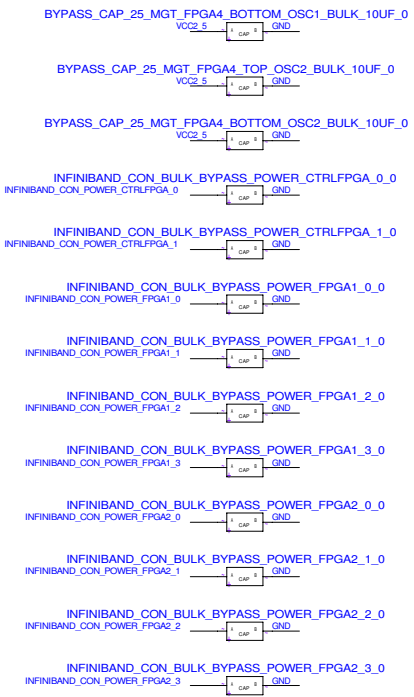
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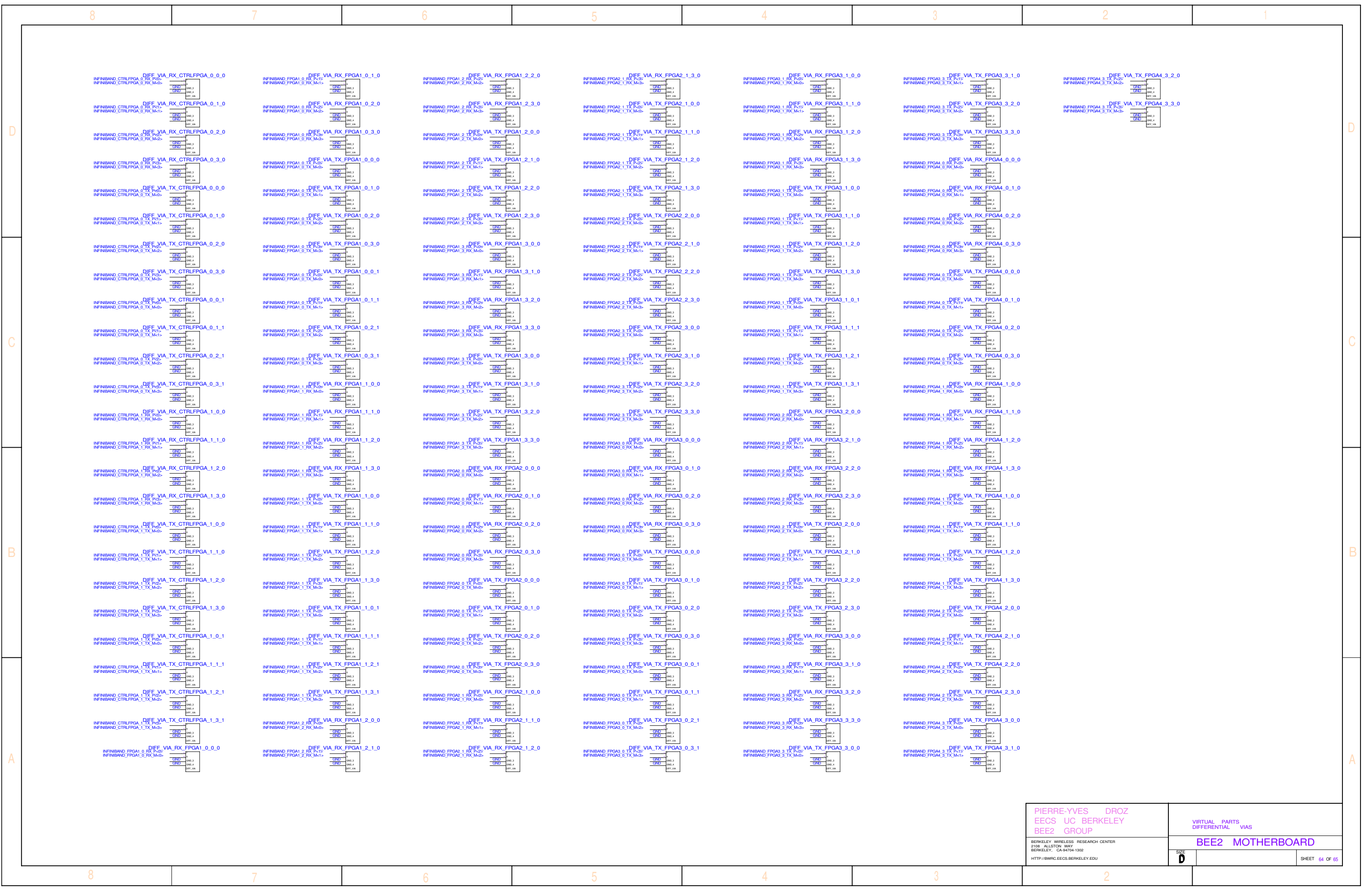
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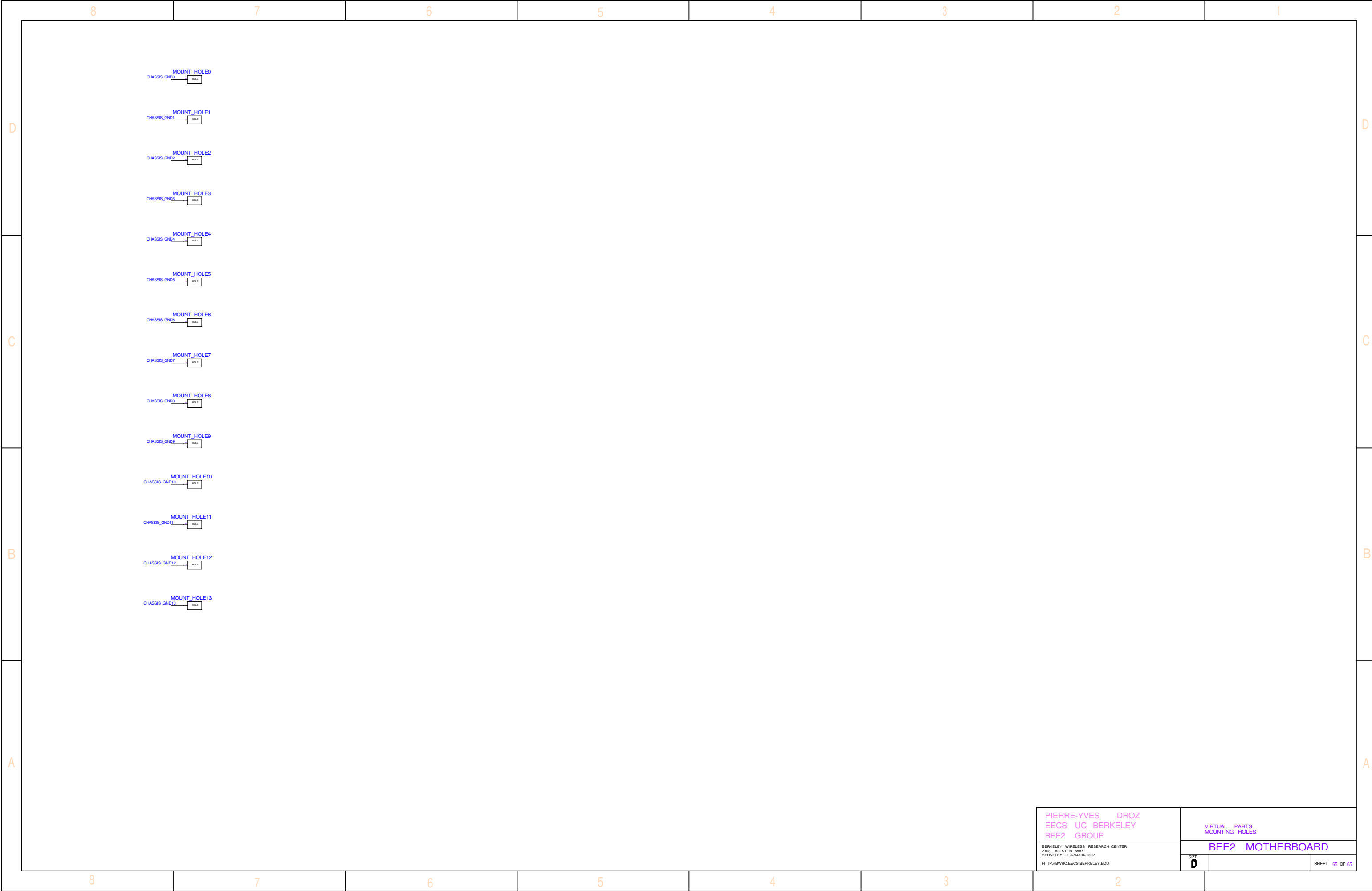
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A

A







PIERRE-YVES DROZ
 EECS UC BERKELEY
 BEE2 GROUP

VIRTUAL PARTS
 MOUNTING HOLES

BEE2 MOTHERBOARD

SIZE
D

SHEET 65 OF 65

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